A CMOS – voltage controlled oscillator with low phase noise

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Abstract—An on chip spiral inductor technique is presented as an efficient method for reducing phase noise of the CMOS-LC Voltage controlled Oscillator (VCO). A simulation-based genetic optimization tool called AMIGO was used to design and simulate the 2.4 GHz VCO in a 0.35-µmCMOS process. This VCO achieves a 25 % tuning range with a control voltage ranging from 0-3.3V, while maintaining a tuning sensitivity of less than 75 MHz/V over the entire frequency range. The simulated single –ended phase noise is – 106 dBc/Hz @ 600 KHz offset frequency when the VCO core is drawing 4.77mA from a 3.3 V supply. The experimental prototype has been fabricated in 0.35 CMOS technology. The measured output spectrum, phase noise and the oscillation frequency are in agreement with the simulation results and the proposed model.

يقدم هذا البحث تصميم ونمذجة وتحليل وقياس مذبذب تحكم جهود ذو ضوضاء بسيطة وذو نتائج متوافقة مع النموذج ويقدم نموذج لضوضاء الوجه ورقم الاستحقاق والذى يعتبر خطى ولكن متغير مع الزمن والدائره الكاملة للمذبذب تم عمل محاكاه لها ومقارنة لنتائج المحاكاه مع نتائج تم قياسها فى ابحاث اخرى. والمذبذب يتميز بأن ضوضاء الوجه قليلة مما ساعد على استخدامه فى تطبيقات كثيرة فى الشبكات اللاسلكية.

Keywords: CMOS-VCO-Low phase noise

1. Introduction

Low phase noise VCO's are an integral part of high performance phase locked loop systems such as frequency synthesizers used in wireless communication systems. On the other hand, the VCO performance in terms of tuning range, phase noise, and power dissipation determines many of basic performance characteristics of a transceiver. The VCO's are widely utilized as clocking source in almost all kinds of transceivers. With growing in demands in broadband data access to internet, carrier frequency for wireless local area networks and Bluetooth technology has been pushed beyond 2.4GHz. In each of these applications, the low cost provided by fully integrated CMOS solution is very attractive. Although relaxation oscillators easily achieve very wide tuning range, their poor phase noise performance is the main drawback [1-3]

CMOS LC-VCO is a superior candidate to achieve low noise for the inherent band pass filtering of LC resonator that can suppress side-band noise. It has allowed for full integration of precise analog filters. The LC VCO is called Harmonic Oscillator because it is capable of producing an almost pure sinusoidal oscillation with good phase noise which represents the phase and frequency fluctuations and spectral purity. It is modeled as a negative resistance oscillator where the tank circuit determines the frequency while the active circuit is called energy restorer [4].

Random fluctuations in the output frequency of the VCO expressed in terms of jitter and phase noise, have a direct impact on the signal-to noise ratio where frequency translation is performed. In particular, RF oscillators employed in wireless transceivers must meet certain phase noise requirements, typically mandating the use of passive LC tanks with a high quality factor (Q). However, the trend towards low cost large-scale integration makes it desirable to implement oscillators monolithically.

Recently, several wideband CMOS LC VCO's have been demonstrated using a variety of techniques. The high intrinsic C_{max} / C_{min} of inversion-or accumulation – type MOS varactors_support a very wide tuning range and their Q is so sufficiently high that good phase noise performance can be determined. [5-6].

The circuit design is given in section II. In section III phase noise modeling is presented, and simulation results are presented in section IV. Measurement results are presented in section V. Finally conclusions are given in section VI.

2. Circuit design

In this paper, a fully differential voltage current - controlled source followed by current mirror as a turbo charger to a fully differential a VCO are proposed. This technique has the benefit of guaranteed start up and well controlled amplitude beside low phase noise and reasonable figure of merit. The amplitude of the resonator will be increased also. Which allows more energy to be stored in the tank circuit, and so it reduces phase noise. Also the tuning range of the spiral inductor is the same as the trapped inductor [7].

2.1. Design constrains

Typical design constraints are assumed regarding power dissipation, bias current, tank amplitude, oscillation frequency, and phase noise as given in table 1.

2.2. Inductor and MOS capacitor

For the low phase noise, design of an inductor with a small L and high quality factor (Q) was the major challenge for the designer. On the other hand, designed MOS capacitors (with drain and source tied together) provides analog frequency tuning with reduced design size. This proved correct approach as an inductor takes more space on chip. It is found out that the best region of operation for optimum Q (so linearity and high Q both obtained), capacitance can be varied by changing the voltage across it. (i.e. control voltage) and center frequency of oscillation can be changed.

2.3. Voltage controlled oscillator

The VCO used in this paper is the complementary cross coupled oscillator, which consists of P-type and N-type MOSFETS, two spiral coils and a two MOSFET capacitors, C_{b1}, C_{b2} employed for switched – band coarse

Table 1
Typical design constrains

Specification	Value
Power dissipated	10mW
Bias current	3 – 5 mA
Tank amplitude (p-p)	< 3.3 V
Oscillation frequency	2.3GHz – 2.45GHz
Phase noise	< -110dBc/Hz @ 600kHz offset

tuning. The PMOS current source which has good phase noise response with respect to the one uses an NMOS pair and where the 1/f noise of PMOS is generally less than for an NMOS with the same dimensions. Fig. 1 shows lossy tank circuit used as a resonator. The Loss is compensated by N and P Channel negative resistance which resulted in better phase noise at a given power dissipation with reduced flicker noise. We also used differential design to suppress substrate noise and simple low noise current source to minimize noise up-conversion. Both P and N type MOSFET's are used to achieve high signal swing and good rise/fall time symmetry. There are several initial design variables associated with this oscillator MOS transistors size, geometric parameters of on-chip spiral inductors (metal spacing, metal width, number of turns, and diameter), maximum value of the varactors, load capacitance and tail bias current in the oscillator core. However the number of design variables can be reduced through proper design considerations.

For example, if we consider the device matching in the cross-coupled topology, one can conclude that these transistors may share the same W and L. Both channel lengthes are set to the minimum feature size allowed by the process technology to reduce parasitic capacitance and achieve the highest trancsconductance. Also for a typical varactor, the ratio is determined by the physics of the capacitance pre specified to represent the next stage loading (0.1 pF). So the independent design variables may reduce to the transistor widths, the spiral inductor parameters, the bias current that controls the tank amplitude, and the maximum capacitance of the varactor.

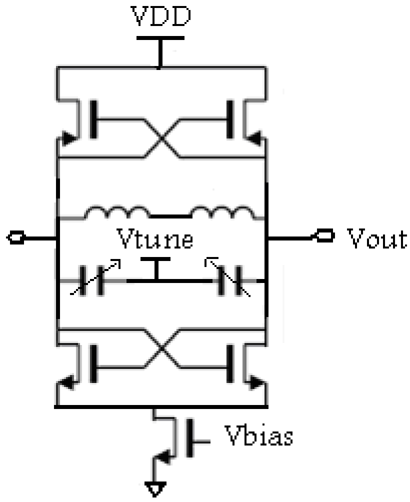

Fig. 1. LC- VCO circuit diagram.

To simplify the optimization process, the on-chip spiral and the varactor are taken out of the optimization process. MOS varactor and spiral macro models are taken from the standard cell library provided by the foundry. The RF macro model for the transistors is also provided by the foundry [8].

The conductance G_m of the tank circuit is

$$G_m = \frac{1}{2}[G_L + G_{VARACTOR} + G_{ds,n} + G_{ds,p}] \; . \qquad (1)$$

Where G_L represents the conductance associated with the coil, $G_{Varacter}$ is the transeconductance of the varactor, and $G_{ds,n}$, $G_{ds,p}$ are the transeconductance of NMOS and PMOS respectively.

The two cross coupled transistors have a gate of one transistor connected to the drain of the other and vice versa and short circuited sources. The conductance seen from the drain is negative, and assuming that the transistors are in saturation, then the equivalent capacitance seen by the drains of the transistors is

$$C_{eq} = 2C_{gd} + \frac{1}{2}[C_{gs} + C_{db} + C_{ds} + C_{gb}] \; . \qquad (2)$$

The main requirement for VCO design is that the tuning range must cover the entire band of operation, phase noise should be minimized at the oscillation frequency and signal power must be high enough to provide the load and circuit power consumption.

In our design these requirements are met since:

The cross coupled transistors work as a negative resistance that sustains oscillation by compensating loss in the LC tank and frequency is controlled by varying the capacitance of the tank

The on-chip spiral inductor is simulated with an Electro Magnetic (EM) simulator ASITIC. The quality factor (Q) can be improved by increasing metal width.

The tranceconductance G_m of the cross-coupled MOS pairs must be high enough to compensate the loss of the tank. The length of the transistor, must be reduced in order to minimize parasitic sources of loss measured by the quality of L (Q_L) and quality of C (Q_c) and the output impedance (G_m) must be larger than the total loss.

Phase noise is an uncertainty of center frequency of VCO output, where the spectrum looks as if it has finite power in certain frequency offset away from the center frequency. In time domain phase noise is referred to as timing jitter [9].

3. LTV- phase noise model

The importance of phase noise in wireless communications comes from the fact that if the local oscillator output contains phase noise, both the down converted and up converted signals in the transceiver will be corrupted. Phase noise is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform as shown in fig. 2 for ideal and actual oscillator.

The spectrum of the phase noise $\phi(t)$ is effectively translated to the oscillation frequency ω_o. The phase noise signal is known as an amplitude modulating sinusoid signal of frequency ω_o that is in turn superimposed on the ideal oscillator itself. An oscillator, however, is a frequency selective circuit and will tend to be out of band if there is a frequency offset from ω_o. Since the impulse response has its maximum value near the zero

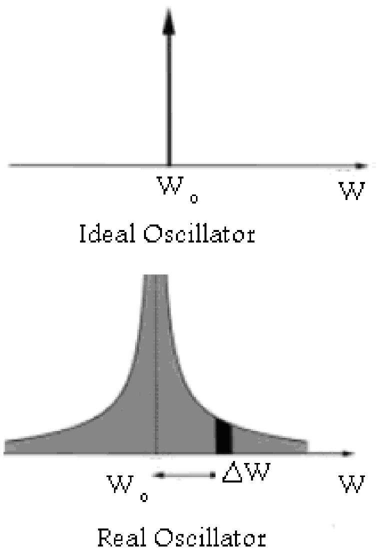

Fig. 2. Illustration of phase noise in frequency domain.

crossing of the oscillator waveform, and a zero value at the maximum, therefore, the LC oscillator is a Linear but Time Varying (LTV) system.

Then the impulse response still completely characterizes the system. The impulse sensitivity function ψ ($\omega_o\tau$) which encodes information about the sensitivity of oscillator to an impulse injected at phase ($\omega_o\tau$) can be expressed as Fourier series:

$$\psi(\omega_o\tau) = \frac{C_o}{2} + \sum_{n=1}^{\infty} C_n \cos\,(n\omega_o\tau + \theta_n)\,. \quad (3)$$

Where the coefficients C_n, are real and θn is the phase of the n^{th} harmonic. On the other hand, an impulsive input produces step change in phase, therefore, the impulse response may be written as:

$$h(t,\tau) = \frac{\psi(\omega_o\tau)}{q_{\max}}\, u(t-\tau)\,, \quad (4)$$

where $u(t)$ is the unit step function and q_{max} is the maximum charge displacement across the capacitor.

The oscillator phase angle change $\Delta\,\Phi$ due to a charge injection Δq into a specific oscillator node at phase angle $\omega_o t$ during the oscillation periods can be written as:

$$\Delta\Phi(t) = \psi(\omega_o\tau)\,\frac{\Delta q}{q_{\max}}\,. \quad (5)$$

Consider a sinusoidal current whose frequency is near an integer multiple m of the oscillator frequency is injected into the system at some frequency and may produce special components at a different frequency, so that :

$$i(t) = I_m \cos[(m\omega_o + \Delta\omega)t]\,. \quad (6)$$

Where $\Delta\omega \ll \omega_o$

$$\phi(t) = \int_{-\infty}^{t\infty} \Delta\phi(t)d\tau\,. \quad (7)$$

We may calculate the excess phase as follows:

$$\phi(t) = \int_{-\infty}^{t} h(t,\tau)\; i(\tau)d\tau\,, \quad (8)$$

when $n = m$, one obtain the following approximation:

$$\phi(t) = \frac{I_m C_m \sin(\Delta\omega t)}{2q_{\max}\Delta\omega}\,. \quad (9)$$

The spectrum of $\Phi(t)$ therefore consists of two equal side bands at $\pm\,\Delta\omega$.

The output voltage may be expressed as:

$$V_{out}(t) = V_m \cos(\omega_o t + \phi(t))\,. \quad (10)$$

This equation may be considered as phase – to –voltage converter.

Assuming a small amplitude disturbances, we find that the power disposed about the carrier is:

$$P(\Delta\omega) \approx 10\;\log\;\left(\frac{I_m\,C_m}{4q_{\max}\Delta\omega}\right)^2, \quad (11)$$

which means that the phase –noise is two sided energy signal. The VCO performance can be compared by means of a figure of merit (FOM), as defined in [11] and may be given by:.

$$VCO_{FOM} = \phi(t)\ dBc/Hz - 20\log\frac{f_{osc}}{f_{offset}} + 10\log\frac{P_{diss}}{1mw}, \quad (12)$$

where f_{osc} is the carrier frequency, f_{offest} is the frequency offset, P_{diss} is the power consumed by the VCO core, and $\phi(t)$ is the phase noise simulated at an offset f_{offest} from the carrier.

The simulated phase noise is -106dBc/Hz at 100 kHz, Offset achieved at an output frequency of 2.73 GHz draws 9mA from 3.3V and supply 29.7mW, which gives a figure of merit of -180.7dBc/Hz.

4. Simulation results

A computer-aided optimization technique has been recently used to find the optimum design for certain LC oscillator topologies in an efficient way. The applied synthesis tool in this study is classified as simulation-based optimization engine based on genetic algorithm AMIGO [8]. Using this tool, we aim to improve the performance of the studied LC VCO.

AMIGO is a simulation-based sizing tool, which provides the best values of the parameters that achieve a specified performance. We specify the devices to be optimized, the device parameters to be manipulated, the interrelation between those parameters and the constraints to be satisfied. The simulator used in the tool is ELDO RFIC. The results obtained from AMIGO represent the best values of the variables that satisfy all design constraints, including the cross-coupled transistor sizes, the bias transistor size, and the bias voltage that maintains the bias transistor in saturation. The used transistors are divided into fingers of maximum width imposed by the technology. These values are shown in table 2.

After optimization, simulation is performed again off line using ELDO RFIC to verify and characterize the performance of the VCO. As shown in table 3, all results meet the performance specifications initially imposed.

Table 2
Synthesized VCO performance summary

Specification	Value
Supply voltage	3.3V
Bias current	4.77ma
Center frequency	2.4GHz
Tuning range	25%
Power dissipation	15.74mW
Tank amplitude (p-p)	3 V
Phase noise (f_c=2.7GHz,@600kHz)	-106 dBc/Hz

Table 3
Models summary of passive Elements

	Parameter	Value
Coil	Inductance	1.717nH
	resistance	2.294 Ohm
	Inductor area	300*300um^2
	Maximum quality factor	6.0@2.2GHz
MOS Varactor	W*L	633.6um*0.65um
	Row*Col	6*16
	C_{min}	0.53pF
	C_{max}	1.96pF
	Minimum quality factor	16.8@2.4GHz
	Maximum quality factor	58.7@2.4GHz

Simulation is performed again offline using ELDO RFIC to verify and characterize the performance of the VCO. All results meet the performance specifications initially imposed. table 4 provides the AMIGO results

The layout of the accumulation – mode MOS varactor is composed of a number of parallel connected small capacitors. It is made up of rows in vertical direction, and columns in horizontal direction. The total width of the varactor is calculated to be equal to (Row*Col* width of a segment). The width of a segment is fixed and equal to 6.6µm [12-13]. Table 5 shows the comparison [3] between our results and similar works.

Table 4
AMIGO Results

Variables	Value
P MOS_W	310µ /11 fingers
N MOS_W	220µ/11 fingers
QL	6@2.2 GHz
Qc	16.8 - 58.7 @2.4GHz

Table 5.
Vco performace comparison

	Harn[3]	This work
Tech. (µm)	0.35	0.35
Center frequency	2.33 GHz	2.4 GHz
I_{bias}	4mA	4.77mA
Phase -noise	-115 dBc/Hz	-107 dBc/Hz
FOM dBc/Hz	175dBc/Hz	180.7dBc/Hz
Tuning range	26%	25%
Power consumption	10mW	15.74mW

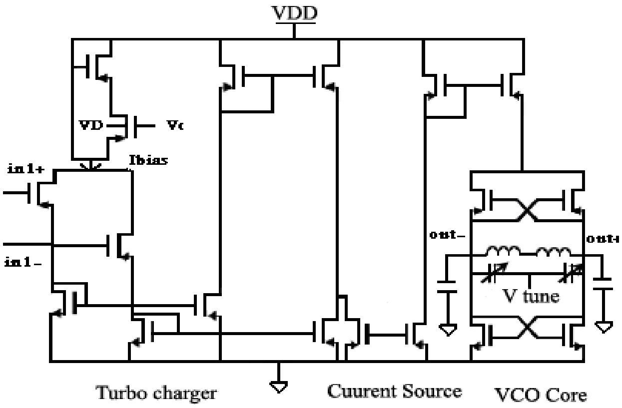

Fig. 3. Core circuit prototype for LC VCO.

5. Experimental results

The Experimental prototype of LC- CMOS -VCO on chip spiral inductor has been fabricated in 0.35 µm CMOS technology. The on chip spiral inductors were realized on a thick top metal layer and have a measured Q ranging from 6 to 8 over the VCO frequency range. The VCO was measured on a test board built on standard FR4 material. A wide tuning range from 1.1 to 2.4 GHz (%25) is achieved with a tuning voltage from 0 to 3.3 V .

Detailed circuit schematic of CMOS LC – VCO is shown in fig. 3, which consider the cross coupled block model and parasitic of the varactor and inductor.

Phase noise measurements were performed using HP5500 phase noise measurement system. Fig. 4 shows the measured phase noise performance.

The measured VCO output spectrum at 2.4GHz is shown in fig. 5. Output power is about -12dBm, which is low due to the losses coming from parasitics.

The measured oscillation frequency against the tuning voltage applied to the gate of the MOS varactor compared with the simulated characteristic is shown in fig. 6.

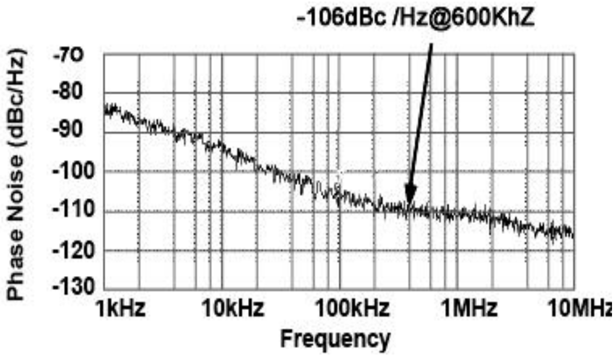

Fig. 4. The measured phase noise against offset frequency.

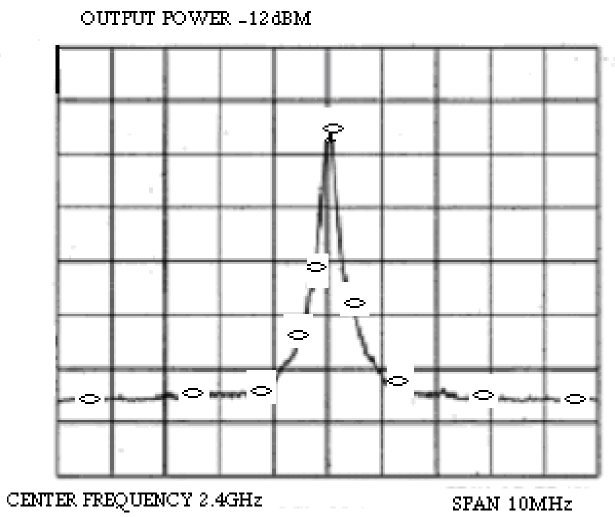

Fig. 5. The output power against the control voltage.

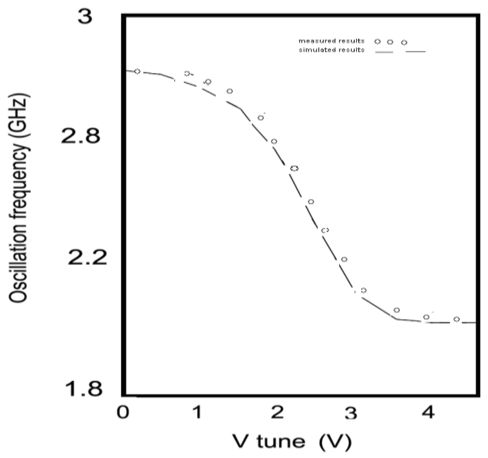

Fig. 6. The Simulated oscillation frequency against offset voltage.

6. Conclusions

New proposed turbo charger VCO has been described. The circuit is guaranteed to start oscillation and provide well-controlled amplitude. The circuit has been simulated and all aspects of its performance have been confirmed. Comparison with published work for the same oscillator topology shows that our design reasonably competes with other work [3], specially for the tuning range. Optimized synthesis for a cross-coupled LC oscillator was demonstrated using a locally developed sizing tool. A 2.4-GHz fully integrated, LC voltage-controlled oscillator (VCO) using AMS 0.33-um MOS transistors is successfully synthesized. The measured phase-noise values are found to be -112, -107, and -106 dBc/Hz at 600-kHz offset from 2.1, 2.4, and 2.7 GHz carriers, respectively. The VCO consume 4.77 mA from a 3.3-V supply. The accumulation-mode MOS varactor tuning is used to achieve 25% of tuning range. The tuning range could also been included in the optimization constraints.

References

[1] M. Alazab, "Wideband CMOS-LC Voltage Controlled Oscillators with Low-Path Noise" Alexandria Engineering Journal, Vol. 46 (6), pp. 1-8 (2007).

[2] Pietro Andreani, et al., "A Study of Phase Noise in Colpitts and LC-tank CNMOS Oscillato", IEEE J. Solid-state Circuits, Vol. 40 (5), pp. 1107-1118 (2005).

[3] D. Harn and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LCVCOs", IEEE, J. Solid-State Giants, Vol. 36, pp. 896-909 (2001).

[4] M. Zannoth, B. Kolb, J. Fenk and R. Weigel, "A Fully Inte Grated VCO at 2 GHz" IEEE, J. Solid- State Giants, Vol. 33, pp. 1987- 1991 (1998).

[5] C. Larn and B. Razavi, "A2,6-GHz/5,2 GHz CMOS Voltage-Controlled Oscillator", in ISSCC Dig. Tech, Papers, pp. 402-403 (1999).

[6] M. Hers Henson, A. Hajimiri, S.S. Mohan, S.p. Boyd and T.H. Lee, "Design and Optimization of LC Oscillators", in Proc. IEEE/ ACM Int. Conf Computer Aided Design, San Jose, CA, pp. 65 – 69 (1999).

[7] M. Alazab, "Design and Simulation of a Wideband CMOS Transcondutance Amplifier", In Proc., URISI, NRSC'99, D6.

[8] Warren. David A. J. Michael Golio and L. Seely, "Large and Small Signal Oscillator Analysis", Microwave Journal, Vol. 32 (5), pp. 229-246 (1989).

[9] A. Hajimiri and T.H. Lee, "Design issues in CMOS Differential LC Oscillators", IEEE J. Solid–State Giants, Vol. 34, pp. 717-724 (1999).

[10] H. Wang. A Hajimiri, and T.H. Lee, "Come Spondence: Comments on Design Issues in CMOS Differential LC Oscillators" IEEE?J, Solid-State Circnts, Vol. 35, pp. 286-287 (2000).

[11] C. De Ranter, G. Van Der Plas, M. Steyaert, G. Gielen and W. Sansen, "CYCLONE: Automated Design and Layout of RFLC- Oscillator", IEEE Trans on Computer-Aide d Design of Integrated Circuits and Systems, Vol. 21, pp. 1161-1170 (2002).

[12] S. Abd El-Khalik, S. Kayed, M.A. Al Azab, M. Dessouky, H.F. Ragai, "Automated Synthesis of Integrated RF CMOS LC VCOs", International Conference on Electrical, Electronic and Computer Engineering (2004).

[13] S.M. Abdel-Khalik "Design Automation of LC Ocillators", Msc. Thesis, Ain Shams University, Egypt (2004).

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