A NEW PARAMETER EXTRACTION TECHNIQUE IN MOSFETS USING SPLIT-ADMITTANCE MEASUREMENTS

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ABSTRACT

A new parameter extraction technique in relatively short channel MOSFETs is presented. The technique is based on a detailed analysis of the gate-substrate and gate-channel admittances, called split-admittances, when applying small-signal gate voltage with different frequencies at different gate biasing conditions. The proposed technique, besides its capability for studying interface trap properties, permits to determine useful device parameters such as the gate oxide thickness, the interfacial doping profile and more important the channel mobility. The channel mobility is extracted using the spilt-admittance data and the device current-voltage transfer characteristics taking into account the interface trap effects. The method is applied to relatively short channel (L<5mm) devices having large aspect ratio (Z/L) to permit easy subthreshold current and admittance measurements. As a result a complete characterization can be carried out by performing direct measurements on a single MOSFET.

keywords: MOSFET, Characterization, Split-Admittance.

I. INTRODUCTION

Performing direct measurements on MOSFETs, in order to accurately extract device parameters is of great interest. This interest becomes a necessity when MOS devices are scaled to small dimensions in VLSI circuits. Increasing down scaling of VLSI devices leads to enhanced electric field intensities which result in the creation of damage at the Si-SiO_2 interface of MOS devices. This in turn accelerates the device aging and degradation mechanisms [1,2].

In literature, several techniques were proposed to study interface trap properties by making direct measurements on relatively short channel MOSFETs [3-7]. However, other device parameters such as the gate oxide thickness, the doping profile and the flat-band voltage are usually determined by performing high frequency C-V measurements on large-area monitor capacitors [8]. The threshold voltage is classically deduced from the I-V transfer characteristics of MOSFETs operating in strong inversion at very small drain voltages [9]. Finally , the effective channel mobility in weak and strong inversion is obtained by combining the high frequency split-capacitance (gate-channel capacitance) data and the device I-V transfer characteristics [10-13]. However, the latter techniques have been always carried out on long and wide channel devices to allow easy capacitance measurements. Also, in those devices, it has been assumed that the channel resistance and the interface trap effects are negligible. A more rigorous model of gate-channel capacitance and conductance in long channel devices was proposed [14] taking into account the effect of channel length on the channel time constant but the influence of the interface traps was still neglected.

At this point it seems important to emphasize the need of performing device characterization on relatively short channel devices with the capability

of introducing the interface trap effects. In this way one could approach the case of typical VLSI devices.

In this paper, we propose a new parameter extraction technique in relatively short channel MOSFETs. The technique is based on a detailed small-signal split-admittance model. The split-admittances, are those measured in the source/drain and in the substrate circuits. The method is capable of extracting interface trap properties, the gate oxide thickness and the doping profile near the Si-SiO_2 interface. The latter is very important to be determined since in VLSI technology the interfacial doping profile is modified to adjust the threshold voltage and to avoid the device punch through. In addition, with the aid of the device I-V transfer characteristics measured at very small drain voltages, the method can be extended to extract the effective channel mobility in subthreshold and strong inversion regions. The method takes into consideration the influence of interface traps on the extracted parameters.

The paper proceeds as follows : In Section II the split-admittance model is formulated starting from the first principles. In Section III the procedure used to extract various device parameters is presented. The experimental details concerning the studied devices and the measuring set-up are described in Section IV. In Section V, the obtained results are presented and discussed emphasizing the sensitivity and accuracy of the method and finally, we state our conclusion in Section VI.

II. *Model of split-Admittance in MOSFET*

In this section, we develop a new model for the split-admittance in short-channel MOSFETs. This model is valid under different bias regimes and provides expressions for gate-substrate and gate-channel admittances as functions of frequency, gate bias and device parameters. We recall the model of split-current in short channel MOSFETs[7] where an arbitrary time varying signal is applied to the gate while the source, drain and substrate are grounded (see Figure (1)). The starting point in our derivation is to show how the split-current densities J_{sub} and $J_{s,d}$, measured in the substrate and source/drain, are related to the applied gate signal $V_g(t)$ and to the hole and electron recombination current densities $J_p(t)$ and $J_n(t)$ through the interface traps. J_{sub} and $J_{s,d}$ have been shown to be expressed as [7] :

$$J_{sub} = C_B \frac{d\varphi_s}{dt} + J_p(t)$$

$$= C_{gb}^{o} \frac{dV_g}{dt} + \left(1 - \frac{C_{gb}^{o}}{C_{ox}}\right) J_p(t) - \frac{C_{gb}^{o}}{C_{ox}} J_n(t) \qquad (1)$$

$$J_{s,d} = C_{inv} \frac{d\varphi_s}{dt} + J_n(t)$$

$$= C_{gc}^{o} \frac{dV_g}{dt} + \left(1 - \frac{C_{gc}^{o}}{C_{ox}}\right) J_n(t) - \frac{C_{gc}^{o}}{C_{ox}} J_p(t) \qquad (2)$$

where C_{ox}, C_{inv} and C_B are the gate oxide, inversion layer and substrate capacitances, respectively, all per unit area and ψ_s is the surface potential. The capacitances C_{gc}^{o} and C_{gb}^{o} are the gate-channel and gate-substrate capacitances, respectively, also per unit area and in the absence of interface traps. These capacitances are given by :

$$C_{gc}^{o} = \frac{C_{ox} C_{inv}}{C_{ox} + C_B + C_{inv}} \; ; \; C_{gb}^{o} = \frac{C_{ox} C_B}{C_{ox} + C_B + C_{inv}} \qquad (3)$$

Generalized expressions for the gate-channel and gate-substrate capacitances will be developed later.

Equations (1) and (2) can be studied in different operating regions depending on $V_g(t)$. In the following analysis we consider the case of an n-channel MOSFET operating either in depletion or in inversion. The applied gate signal is a small alternating voltage (<kT/q) superimposed on a d.c. voltage determining the device operating region.

II. 1 *Depletion:*

When the device is biased in depletion, there is a weak interaction between the interface traps and the minority carrier band (conduction band) and consequently J_n can be neglected compared to J_p. Also, in depletion $G_{gc}^{o} = 0$. Hence, eqns (1) and (2) can be rewritten as:

$$J_{sub} \approx C_{gb}^{o}\frac{dV_g}{dt}+\left(1-\frac{C_{gb}^{o}}{C_{ox}}\right)J_p(t)\ ;\ J_{s,d}\approx 0 \qquad (4)$$

Assuming a sinusoidal variation for $V_g(t)$, the amplitude of the resulting alternating component of J_{sub} is given by :

$$\tilde{J}_{sub}=J\omega C_{gb}^{o}\tilde{V}_g+\left(1-\frac{C_{gb}^{o}}{C_{ox}}\right)\tilde{J}_p \qquad (5)$$

where $\tilde{V}_g$ and $\tilde{J}_p$ are the amplitudes of the a.c. components of $V_g(t)$ and $J_p(t)$, respectively, and ω is the operating angular frequency.

Defining the admittance per unit area $Y_{it,p}$, of the interface traps interacting with the majority carrier band (valence band) as :

$$Y_{it,p}=\frac{\tilde{J}_p}{\tilde{\varphi}_s} \qquad (6)$$

where $\tilde{\varphi}_s$ is the amplitude of the a.c. component of the semiconductor surface potential, eqn (5) can be rewritten as :

$$\tilde{J}_{sub}=j\omega C_{gb}^{o}\tilde{V}_g+\left(1-\frac{C_{gb}^{o}}{C_{ox}}\right)Y_{it,p}\tilde{\varphi}_s \qquad (7)$$

The relationship between $\tilde{\varphi}_s$ and $\tilde{V}_g$ can be shown to be expressed as:

$$\tilde{\varphi}_s=\frac{C_{ox}}{C_B+C_{ox}+\dfrac{Y_{it,p}}{j\omega}}\tilde{V}_g \qquad (8)$$

and eqn (7) becomes

$$\tilde{J}_{sub}=j\omega C_{gb}^{o}\tilde{V}_g+\left(1-\frac{C_{gb}^{o}}{C_{ox}}\right)\frac{C_{ox}Y_{it,p}}{C_B+C_{ox}+\dfrac{Y_{it,p}}{j\omega}}\tilde{V}_g \qquad (9)$$

We define the gate-substrate admittance Y_{gb} per unit area as:

$$Y_{gb}=\frac{\tilde{J}_{sub}}{\tilde{V}_g}=G_{gb}+j\omega C_{gb} \qquad (10)$$

where G_{gb} and C_{gb} are the generalized gate-substrate conductance and capacitance per unit area, respectively, taking into account the presence of interface traps. Also, the interface trap admittance $Y_{it,p}$ can be put in the form :

$$Y_{it,p}=G_{pp}+j\omega C_{pp} \qquad (11)$$

where G_{pp} and C_{pp} are the parallel conductance and capacitance per unit area of interface traps interacting with the valence band. Making use of eqns (9)-(11) we get

$$G_{gb}=\frac{\omega^2 C_{ox}^2 G_{pp}}{G_{pp}^2+\omega^2(C_B+C_{ox}+C_{pp})^2} \qquad (12)$$

and,

$$C_{gb}=C_{gb}^{o}+\frac{(C_{ox}-C_{gb}^{0})\left[G_{pp}^2+\omega^2 C_{pp}(C_B+C_{ox}+C_{pp})\right]}{G_{pp}^2+\omega^2(C_B+C_{ox}+C_{pp})^2} \qquad (13)$$

Equations (12) and (13) provide general expressions for the gate - substrate conductance and capacitance per unit area in depletion taking into account the interface trap effects. If the interface traps are not present, G_{gb} goes to zero and C_{gb} is given by C_{gb}^{o}.

Having reached generalized expressions for G_{gb} and C_{gb} in depletion, it is advantageous from the point of view of parameter extraction and device characterization to deduce the inverse relations in which the interface trap and device parameters are explicitly expressed in terms of the measured admittances. Manipulating eqns (12) and (13), expressions for G_{pp} and C_{pp} can be obtained in terms of G_{gb} and C_{gb} as:

$$\frac{G_{pp}}{\omega C_{ox}}=\frac{\omega C_{ox}G_{gb}}{G_{gb}^2+\omega^2(C_{ox}-C_{gb})^2} \qquad (14)$$

and,

$$\frac{C_{pp}+C_B}{C_{ox}} = \frac{(C_{ox}-C_{gb})C_{gb}\,\omega^2 - G_{gb}^2}{G_{gb}^2+\omega^2(C_{ox}-C_{gb})^2} \qquad (15)$$

II.2 *Inversion*

When the device is biased in weak or strong inversion, there is a weak interaction between the interface traps and the valence band. Consequently, $J_p(t)$ can be neglected compared to $J_n(t)$. Also, in inversion $C_{gc} \neq 0$ and specifically in weak inversion $C_{gb} \neq 0$

Hence, eqns (1) and (2) can be rewritten as :

$$J_{sub} = C_{gb}^{0}\frac{dV_g}{dt} - \frac{C_{gb}^{o}}{C_{ox}}J_n(t), \qquad (16)$$

and,

$$J_{s,d} = C_{gc}^{o}\frac{dV_g}{dt} + \left(1-\frac{C_{gc}^{o}}{C_{ox}}\right)J_n(t) \qquad (17)$$

Proceeding in the same way as we have done in depletion, the amplitudes of the alternating components of J_{sub} and $J_{s,d}$ can be obtained as:

$$\tilde{J}_{sub} = j\omega\, C_{gb}^{o}\tilde{V}_g - \frac{C_{gb}^{o}}{C_{ox}}Y_{it,n}\tilde{\varphi}_s \qquad (18)$$

$$\tilde{J}_{s,d} = j\omega\, C_{gc}^{o}\tilde{V}_g + \left(1-\frac{C_{gc}^{o}}{C_{ox}}\right)Y_{it,n}\tilde{\varphi}_s \qquad (19)$$

where $Y_{it,n} = \dfrac{\tilde{J}_n}{\tilde{\varphi}_s}$ being the admittance per unit area of the interface traps interacting with the conduction band. Also, we can show that $\tilde{\varphi}_s$ is related to $\tilde{V}_g$ by:

$$\tilde{\varphi}_s = \frac{C_{ox}\tilde{V}_g}{C_B + C_{inv} + C_{ox} + \dfrac{Y_{it,n}}{j\omega}} \qquad (20)$$

Defining the gate-channel admittance Y_{gc} per unit area as :

$$Y_{gc} = \frac{\tilde{J}_{s,d}}{\tilde{V}_g} = G_{gc} + j\omega C_{gc} \qquad (21)$$

where G_{gc} and C_{gc} are the generalized gate-channel conductance and capacitance per unit area, respectively. Putting $Y_{it,n}$ in the form

$$Y_{it,n} = G_{pn} + j\,\omega\, C_{pn} \qquad (22)$$

where G_{pn} and C_{pn} are the parallel conductance and capacitance per unit area respectively of interface traps interacting with the conduction band, we can obtain expressions for G_{gb} , C_{gb}, G_{gc} and C_{gc} as:

$$G_{gb} = \frac{-\omega^2 C_{ox} C_B G_{pn}}{G_{pn}^2 + \omega^2(C_B + C_{inv} + C_{ox} + C_{pn})^2} \qquad (23)$$

$$C_{gb} = \frac{\omega^2 C_{ox} C_B (C_B + C_{inv} + C_{ox} + C_{pn})}{G_{pn}^2 + \omega^2(C_B + C_{inv} + C_{ox} + C_{pn})^2} \qquad (24)$$

$$G_{gc} = \frac{\omega^2 C_{ox} G_{pn} (C_{ox} + C_B)}{G_{pn}^2 + \omega^2(C_B + C_{inv} + C_{ox} + C_{pn})^2} \qquad (25)$$

$$C_{ox} - C_{gc} = \frac{\omega^2 C_{ox}(C_B + C_{ox})(C_B + C_{inv} + C_{ox} + C_{pn})}{G_{pn}^2 + \omega^2(C_B + C_{inv} + C_{ox} + C_{pn})^2} \qquad (26)$$

Equations (23) - (26) provide general expressions for the split-conductances and capacitances per unit area in weak inversion ($C_{gb}^{o} \neq 0$) taking into account the interface trap effects. If the interface traps are not present both conductances (G_{gb} and G_{gc}) go to zero whereas $C_{gb} = C_{gb}^{o}$ and $C_{gc} = C_{gc}^{o}$, which are known as the split-capacitances of Koomen [15].

It is interesting to note that G_{gb} (eqn (23)) is negative ; this is attributed to the reflection of G_{pn} through the capacitive coupling components of the device into the substrate circuit. Moreover, since in weak inversion C_B is a slowly varying function of gate bias and C_{inv} is still smaller than or comparable to C_B, we expect that at a given operating frequency, G_{gb} exhibits a negative peak depending on G_{pn} as a function of the gate bias. This result is verified experimentally in section V.

The total conductance G_g can be obtained by adding up eqns (23) and (25) whereas the total capacitance C_g is obtained by adding eqns (24) - (26). So we can show that

$$G_g=G_{gb}+G_{gc}=\frac{\omega^2 C_{ox}^2 G_{pn}}{G_{pn}^2+\omega^2(C_B+C_{inv}+C_{ox}+C_{pn})^2} \quad (27)$$

$$C_{ox}-C_g=C_{ox}-(C_{gb}+C_{gc})=\frac{\omega^2 C_{ox}^2(C_B+C_{inv}+C_{ox}+C_{pn})}{G_{pn}^2+\omega^2(C_B+C_{inv}+C_{ox}+C_{pn})^2} \quad (28)$$

Manipulating eqns (27) and (28) we can obtain expressions for G_{pn} and C_{pn} in terms of G_g and C_g as:

$$\frac{G_{pn}}{\omega}=\frac{\omega C_{ox}^2 G_g}{G_g^2+\omega^2(C_{ox}-C_g)^2}, \quad (29)$$

$$\frac{C_{pn}+C_B+C_{inv}}{C_{ox}}=\frac{\omega^2 C_g(C_{ox}-C_g)-G_g^2}{G_g^2+\omega^2(C_{ox}-C_g)^2} \quad (30)$$

In the next section we shall demonstrate how to extract important device parameters from the split-admittance data using eqns (23) - (26). The device parameters of interest are the gate oxide capacitance, the semiconductor bulk capacitance and consequently the interfacial doping profile. Moreover, eqns (14) and (29) can be used to study interface trap properties in depletion and in weak inversion, respectively. Finally, eqn (30) can be used to obtain the inversion layer capacitance and with the aid of the device I-V transfer characteristics, the effective channel mobility can be determined.

III. *Method of Parameter Extraction*

III. 1. *Interface Trap Properties*

The interface trap properties in depletion and in weak inversion have been studied extensively [6]. Interface trap density profile and interface trap capture cross-sections for electrons and holes throughout the semiconductor band gap have been obtained assuming that the interface trap statistical model [8], which takes into account the surface potential fluctuations, is valid. In our present technique, G_g and C_g, in depletion, are simply G_{gb} and C_{gb} given by eqns (12) and (13) respectively (note that $G_{gc}= 0$ and $C_{gc}= 0$, in depletion) and the interface trap properties can be extracted using eqn (14). In weak inversion, G_g and C_g are given by eqns (27) and (28) and the interface trap properties can be determined using eqn (29).

III.2. *Gate Oxide Layer Capacitance*

The gate oxide layer capacitance C_{ox} and consequently the gate oxide thickness are often determined from high frequency C-V measurements performed on a large area on-chip monitor MOS capacitors.

The measured MOS capacitance is simply (neglecting the interface trap effects) the series combination of C_{ox} and C_B. In strong accumulation C_B is much greater than C_{ox} and consequently the measured capacitance is equal to C_{ox} with a high degree of accuracy. However, for MOS devices with thin (~10nm) gate oxide layers, C_{ox} becomes a large quantity and may be comparable to C_B in strong accumulation. As a result, the measured capacitance increases slowly as a function of V_g and large values of V_g must be used for accurate C_{ox} measurements. Furthermore, at high frequencies, if the substrate series resistance is not neglected, the measured MOS capacitance in strong accumulation decreases. Hence, erroneous values of C_{ox} may be obtained and a correction for the series resistance must be included [8]. In our method, C_{ox} can be determined independently from the split-admittance data in weak inversion. Making use of eqns (23) - (26), we can show that

$$\frac{G_{gb}}{G_{gc}}=-\frac{C_B}{C_B+C_{ox}}, \quad (31)$$

and,

$$\frac{C_{gb}}{C_{ox}-C_{gc}}=\frac{C_B}{C_B+C_{ox}} \quad (32)$$

from which C_{ox} and C_B can be obtained in terms of the split conductances and capacitances.
Doing so we get

$$C_{ox} = C_{gc} - C_{gb}\frac{G_{gc}}{G_{gb}}, \qquad (33)$$

and,

$$C_B = -C_{ox}\frac{G_{gb}}{G_{gc}+G_{gb}} \qquad (34)$$

C_{ox} is determined using eqn (33) and then used in eqn (34) to obtain C_B. In section V, we will show that by varying V_g and the operating frequency f, sensitive measurements and accurate determination of C_{ox} and $C_B(V_g)$ can be achieved.

III.3 *Doping Profile*

Classically, doping profiling is performed by carrying out combined high and low frequency capacitance measurements on large area MOS capacitors. An exploration of a wider range of depth below the semiconductor surface can be performed by applying the pulse method [8]. In the present method, depth profiling of the doping concentration is directly done on MOSFETs using the split-admittance data in depletion and in weak inversion.

III.3.1 *Depletion*

In depletion, doping profiles can be constructed in an identical manner as done using the high-low frequency capacitance method. In this case, since both G_{gc} and C_{gc} are zero, the total gate capacitance and conductance are simply C_{gb} and C_{gb}, respectively, and hence, the doping profile $N_a(W)$ can be shown to be expressed as [8]:

$$N_a(W) = 2\,\frac{(1-C_{gb,L}/C_{ox})}{(1-C_{gb,H}/C_{ox})}\left[q\varepsilon_s\frac{d}{dV_g}\left(\frac{1}{C_{gb,H}}\right)^2\right]^{-1} \qquad (35)$$

where $C_{gb,L}$ and $C_{gb,H}$ are the low and high frequency gate-substrate capacitances, respectively, ε_s is the semiconductor, permittivity and W is the depletion layer width expressed as :

$$W = \varepsilon_s\left(\frac{1}{C_{gb,H}} - \frac{1}{C_{ox}}\right) \qquad (36)$$

III.3.2 *Weak Inversion*

In weak inversion, slow changes in the gate charge density are balanced not only by changes in the bulk charge Q_B and the interface trap charge Q_{it} but also by a change in the inversion charge Q_{inv}, particularly when Q_{inv} becomes comparable to Q_B (onset of strong inversion). Moreover, due to the fast response of the channel in short channel devices, both the high and low frequency capacitance measurements are affected by C_{inv}. Therefore, an analogous expression for $N_a(W)$ like that of eqn (35) is not valid in weak and strong inversion modes. However, in the present technique, since C_B can be extracted separately from the split-admittance data the doping profile can be easily determined as follows : assuming that the depletion approximation is valid, C_B can be expressed as :

$$C_B = \frac{dQ_B}{d\varphi_s} = qN_a(W)\frac{dW}{d\varphi_s} \qquad (37)$$

with dW expressed as :

$$dW = \varepsilon_s d\left(\frac{1}{C_B}\right) \qquad (38)$$

Hence, C_B can be rewritten as:

$$C_B = q\varepsilon_s N_a(W)\frac{d}{dV_g}\left(\frac{1}{C_B}\right)\cdot\frac{dV_g}{d\varphi_s} \qquad (39)$$

The quantity $\frac{d\varphi_s}{dV_g}$ can be shown to be expressed as:

$$\frac{d\varphi_s}{dV_g} = \frac{C_{ox}}{C_B + C_{inv} + C_{ox} + C_{it}} \qquad (40)$$

where $C_{it} = \frac{dQ_{it}}{d\varphi_s} = qD_{it}$ is the interface trap capacitance per unit area ; D_{it} being the interface trap density in $eV^{-1}\,cm^{-2}$. The right hand side of eqn. (40) is simply given by:

$$\frac{C_{ox}}{C_B + C_{inv} + C_{ox} + C_{it}} = 1 - \frac{C_{gL}}{C_{ox}} = 1 - \frac{1}{C_{ox}}(C_{gb,L} + C_{gc,L}) \qquad (41)$$

where, C_{gL}, $C_{gb,L}$, and $C_{gc,L}$ are the low frequency total gate capacitance, gate-substrate capacitance and gate-channel capacitance, all per unit area, respectively.

Making use of eqns (39) - (41) $N_a(W)$ can be shown to be expressed as :

$$N_a(W) = 2\left[1-\frac{(C_{gb,L}+C_{gc,L})}{C_{ox}}\right]\left[q\varepsilon_s\frac{d}{dV_g}\left(\frac{1}{C_B^2}\right)\right]^{-1} \quad (42)$$

with W simply given by:

$$W = \frac{\varepsilon_s}{C_B} \quad (43)$$

III.4 *Channel Mobility*

The two most commonly used techniques for measuring the MOSFET effective channel mobility are, the d.c. current method [16] and the split-capacitance method [10]-[13]. The d.c. drain current method is applicable in devices operating in strong inversion and results in inaccurate values of channel mobility in weak inversion (subthreshold region). The spilt-capacitance method however, is applicable in strong inversion and in weak inversion as well. In this method, it has been found that in order to avoid the interface trap effects, the spilt-capacitance measurements should be carried out at sufficiently high frequencies. Commonly, the inversion layer charge per unit area Q_{inv} is obtained as a function of the gate bias using :

$$Q_{inv}(V_g) = \int_{-\infty}^{V_g} C_{gc,H}(V')\,dV' \quad (44)$$

where $C_{gc,H}$ is the high frequency gate-channel capacitance per unit area.

The effective channel mobility $\mu(V_g)$ can be obtained from the drain current I_d (V_g) transfer characteristics, at very small drain voltage V_d, as:

$$\mu(V_g) = \frac{I_d(V_g)}{(Z/L)V_d Q_{inv}(V_g)} \quad (45)$$

where Z and L are the effective channel width and length, respectively. The ratio Z/L is commonly known as the device aspect ratio. As noted in [13], despite the marked improvement over the d.c. drain current technique, the high frequency split capacitance method still has one problem. The $Q_{inv}(V_g)$ values are obtained using eqn (44) with V_d=0 (source, drain and substrate are grounded) and then substituted in eqn (45) to obtain $\mu(V_g)$. However, for accurate results of $\mu(V_g)$, the inversion charge must be evaluated for the same value of V_d at which the $I_d(V_g)$ measurements are performed. It has been suggested that as long as I_d is measured with $V_d << kT/q$, the error in the obtained results is insignificant. Experimentally, it is observed that when $V_d << kT/q$, the measured $I_d(V_g)$ becomes noisy, particularly in the subthreshold region where very small currents have to be measured. For this reason, a typical range of V_d ~40 - 100 mV (significantly greater than kT/q at room temperature) has been widely used in literature for the drain current measurements. Therefore, an experimental procedure to enable accurate determination of $Q_{inv}(V_g)$ at any finite V_d value has been proposed [13].

In the present technique, the problem of noisy drain currents in the subthreshold region when $V_d << kT/q$ can be avoided by increasing the device aspect ratio (Z/L), that is by using test devices having large channel widths and relatively short channel lengths. This arrangement has many advantages: first, it allows noiseless subthreshold current measurements even with values of $V_d << kT/q$. Second, it permits easy admittance measurements by keeping a large reasonable effective channel area. Third, performing measurements on relatively short channel devices renders the channel resistance and consequently the channel time constant limitation [6] negligible. This is very important particularly, when measurements are carried out at very high frequencies. Finally, since relatively short channel devices are used, direct characterization of typical VLSI devices is performed instead of conventional characterization using large area MOS devices. Taking all the previous remarks into consideration, we can conclude that eqns (44) and (45) can be used to obtain accurately $\mu(V_g)$ provided that $V_d << kT/q$. However, another problem may arise concerning $Q_{inv}(V_g)$ determined using eqn (44). The high frequency gate-channel

capacitance $C_{gc,H}$ may be affected by the interface traps particularly near the onset of strong inversion. In this case the interface traps near the minority carrier band edge (bottom of the conduction band) may respond to the a.c. signal. Therefore, very high frequencies have to be used which may in turn, impose a problem concerning the channel time constant. The interface trap effects have never been considered so far in any of the proposed techniques used for channel mobility determination. This could be important when characterizing aged and degraded VLSI devices, where a significant increase in the interface trap density and consequently mobility degradation could take place.

In the present method, the split-admittance data can be used to extract the purified (without interface trap effects) gate-channel capacitance $C_{gc,p}$ which must be introduced in eqn. (44) in place of $C_{gc,H}$ to evaluate accurately $Q_{inv}(V_g)$. The proposed procedure is as follows : Equation (30) relates C_{pn} , C_B and C_{inv} to the total gate capacitance C_g and conductance G_g at a given value of V_g and a frequency f. As discussed in section III. 2, $C_B(V_g)$ can be determined from the split-admittance data. On the other hand, $C_{pn}(V_g,\omega)$ can be determined from the $G_{pn}(V_g,\omega)/\omega$ data using the statistical interface trap model [8] which accounts for the surface potential fluctuations. Finally, $C_{inv}(V_g)$ can be extracted using eqn. (30). The purified gate-channel capacitance $C_{gc,p}(V_g)$ per unit area is then simply calculated as :

$$C_{gc,p} = \frac{C_{ox} C_{inv}(V_g)}{C_B(V_g) + C_{inv}(V_g) + C_{ox}} \qquad (46)$$

which can be used in eqn. (44) to evaluate accurately $Q_{inv}(V_g)$.

IV. EXPERIMENTAL DETAILS

The devices used in this study are poly-silicon n-channel MOSFETs having an average substrate doping density $N_a = 2x10^{16}$ cm^{-3}, average gate-oxide thickness t_{ox} = 25 nm, channel length L=3 μm and channel width Z = 6000 μm. As mentioned in section III.4 relatively short channel devices, having large aspect ratio, have been used. The average substrate doping is determined using the maximum-minimum high frequency capacitance method [8] performed on large-area on-chip capacitors. The average gate oxide thickness is deduced from ellipsometry and confirmed by high-frequency C-V measurements carried out on the mentioned monitor capacitors.

In order to demonstrate the potential of the proposed technique for extracting various device parameters, particularly the effective channel mobility, even in the presence of relatively high interface trap densities, the devices under test were electrically stressed using Fowler-Nordheim stress.

Split-admittance measurements were carried out at room temperature using the HP4192A LCR meter in the frequency range between 50 kHz and 10 MHz. At lower frequencies, (50Hz $\leq$ f $\leq$ 50 kHz) the PAR-124A synchronous detector equipped with the PAR-184 current/voltage converter was used. A schematic diagram of the measuring circuit is shown in Figure (1). Further details of the experimental procedure including correction of the split-capacitances for the overlap and parasitic capacitances are discussed elsewhere [6]. The I-V transfer characteristics are obtained using the HP 4145 Semiconductor Parameter Analyzer. The threshold voltage V_T is obtained from the I-V transfer characteristics by extrapolation [9]. A threshold voltage value of about 0.72 V is typically obtained (see Figure (7)).

V. RESULTS AND DISCUSSION

As an illustration, Figure (2) shows the obtained split-admittance curves as functions of the gate bias at two different frequencies (50 kHz and 1 MHz). Figures (2-a) and (2-b) represent the measured (or total) gate-channel conductance $G_{gc,t}$ and capacitance $C_{gc,t}$ while Figures (2-c) and (2-d) show the total gate-substrate conductance $G_{gb,t}$ and capacitance $C_{gb,t}$. It is seen that at a given frequency, $G_{gc,t}(V_g)$ exhibits a conductance peak attributed to the interaction of interface traps with the minority carrier band (conduction band) [6]. This peak shifts towards strong inversion with increasing frequency. On the other hand however, $G_{gb,t}(V_g)$ exhibits two distinct peaks : a positive peak in depletion and a negative one in weak inversion. The positive peak is attributed to the interaction of interface traps with the majority carrier band (Valence band). This peak

shifts towards accumulation with increasing frequency and is classically used to characterize interface traps in the lower half of the semiconductor band gap [6]. The negative conductance peak in weak inversion is attributed to the influence of interface traps reflected into the substrate circuit through the capacitive coupling of C_{ox} and the nonvanishing $C_B(V_g)$. This confirms the split-admittance model discussed in section II. It is interesting to note that by adding up $G_{gb,t}$ and $G_{gc,t}$ the total gate conductance $G_{g,t}$ is obtained and is characterized by two positive distinct peaks as noted in [6].

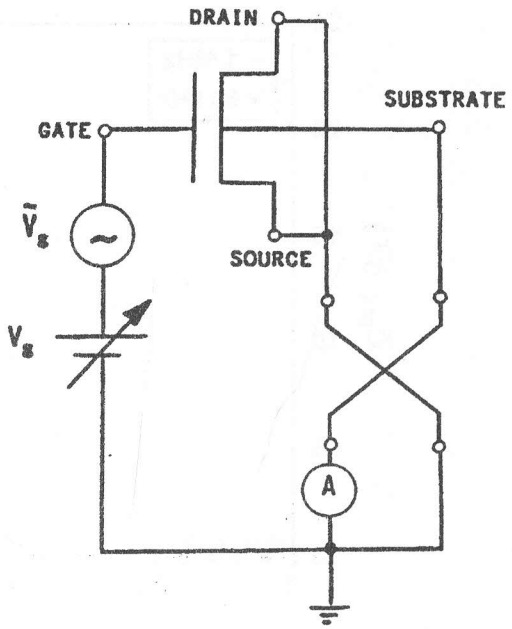

Figure 1. Schematic diagram for the split-admittance measuring circuit.

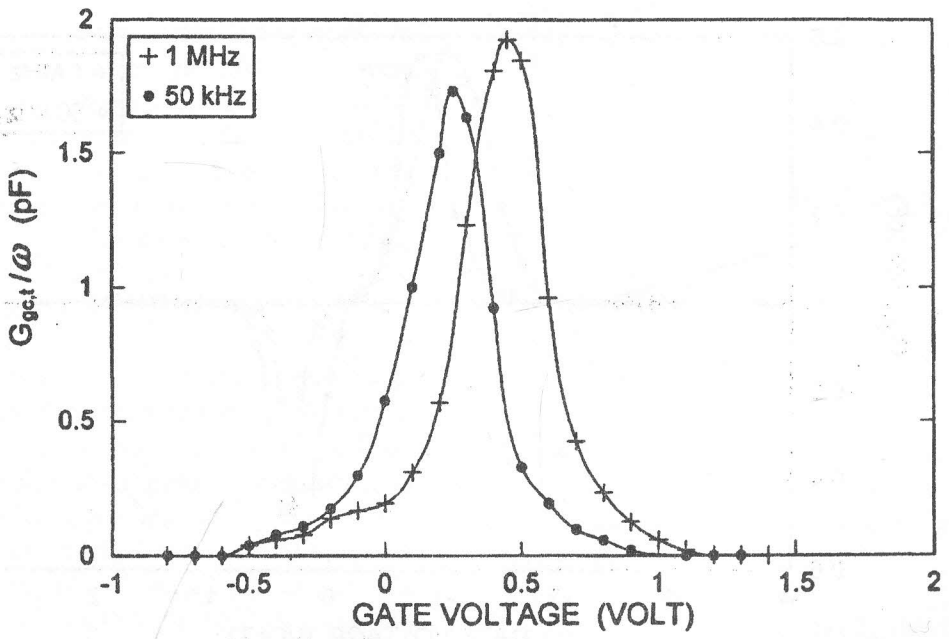

Figure 2a. Measured gate-channel conductance versus gate bias for a transistor of L=3 μm at f = 50 kHz and 1 MHz.

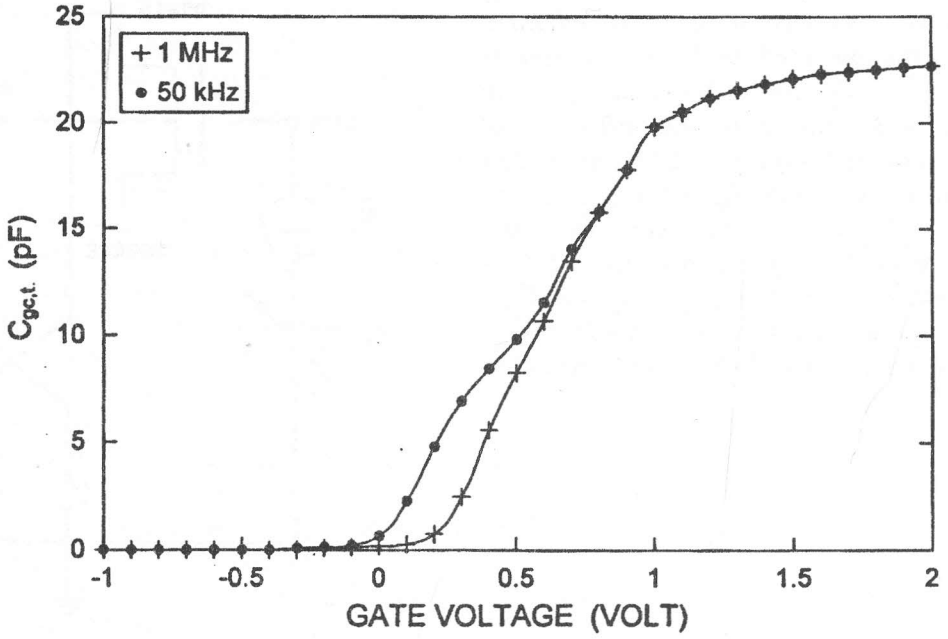

Figure 2b. Measured gate-channel capacitance versus gate bias for a transistor of L=3 μm at f = 50 kHz and 1 MHz.

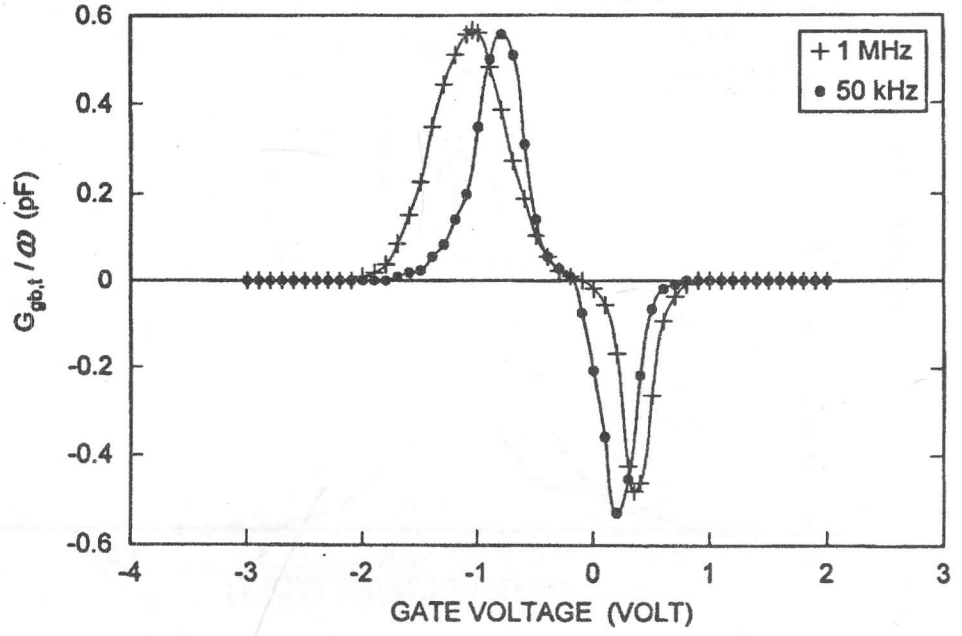

Figure 2c. Measured gate-substrate conductance versus gate bias for a transistor of L=3 μm at f = 50 kHz and 1 MHz.

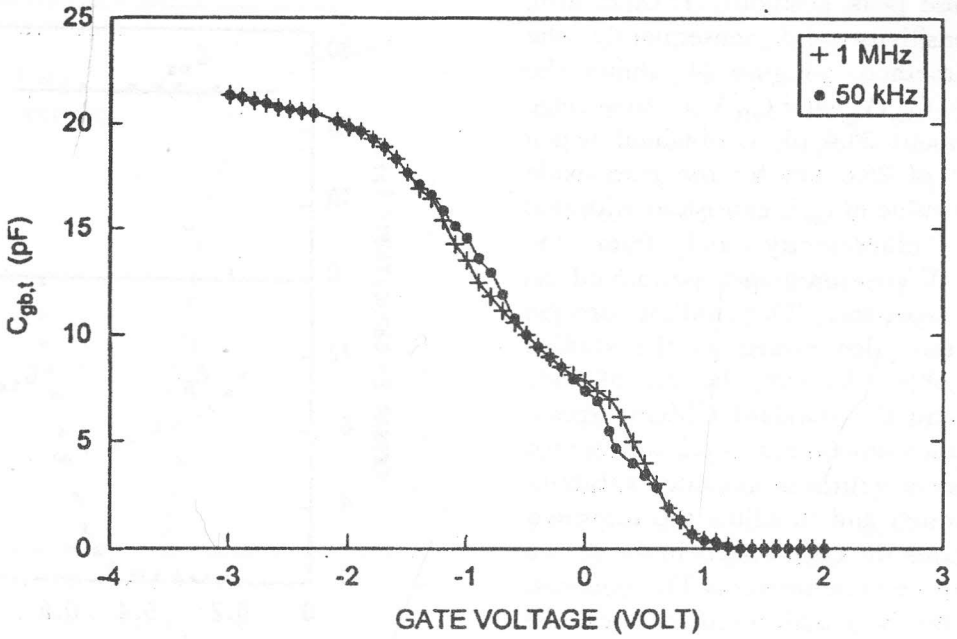

Figure 2d. Measured gate-substrate capacitance versus gate bias for a transistor of L=3 μm at f = 50 kHz and 1 MHz.

Also the split-capacitances are influenced by interface traps. For a given gate bias in weak inversion $C_{gc,t}$ increases with decreasing frequency as a result of the interface trap response to the a.c. signal. Similarly, for a given gate bias in depletion $C_{gb,t}$ increases with decreasing frequency. However, in weak inversion $C_{gb,t}$ decreases with decreasing frequency which is attributed, as mentioned previously, to the reflection of interface traps into the substrate circuit.

The parameter extraction procedure is started by determining the interface trap properties (interface trap density profile $D_{it}(E)$ and capture cross-sections σ_n and σ_p) using the total gate-admittance data. The details of the interface trap study throughout the semiconductor band gap have been extensively discussed elsewhere [6]. Figure (3) shows the obtained results of $D_{it}(E)$, $\sigma_n(E)$ and $\sigma_p(E)$. Relatively high values of D_{it} ($\sim 10^{11}$ eV^{-1} cm^{-2}) are obtained as a result of the electrical stress carried out on the studied devices. However, lower interface trap densities, ($<10^{10}$ eV^{-1} cm^{-2}) can be easily detected with good accuracy using this technique.

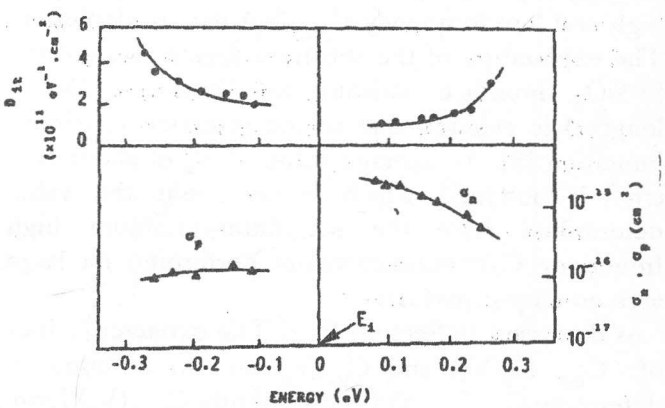

Figure 3. Energy profiles of the interface trap density and the capture cross sections for electrons and holes as obtained using gate-admittance measurements.

As discussed in Section III.2, the total gate oxide capacitance C_{ox} and the total bulk capacitance $C_B(V_g)$ can be determined from the split-admittance data in weak inversion using eqns (33) and (34). Since both $G_{gc}(V_g)$ and $G_{gb}(V_g)$ exhibit peaks at specified values of V_g depending on the operating frequency, it is advantageous to determine $C_{ox}(V_g)$

and $C_B(V_g)$ at those peak positions. This, in turn, increases the sensitivity and consequently the accuracy of the method. Figure (4) shows the obtained results for $C_{ox}(V_g)$ and $C_B(V_g)$. An average value of C_{ox} of about 24.4 pF is obtained which results in a value of 25.6 nm for the gate oxide thickness t_{ox}. This value of t_{ox} is consistent with that obtained from ellipsometry and from the high-frequency C-V measurements performed on large-area on-chip capacitors. This confirms also the assumption that the edge effects in the studied devices are negligible. In fact, the use of wide channel devices, and the standard CMOS process which includes shallow-implanted (~ 0.2 mm) source and drain junctions and a surface-implanted substrate to avoid punchthrough and to adjust the threshold voltage, all minimizes the edge effects in the device current and admittance measurements.The obtained results of $C_B(V_g)$ can be readily used to determine the interfacial substrate doping profile $N_a(W)$. The results are shown in Figure (5). The lower part (filled circles) of the profile is obtained from the $C_B(V_g)$ data in weak inversion using eqn (42), while the upper part (empty circles) is obtained from the high and low frequency $C_{gb,t}(V_g)$ data in depletion. The exploration of the substrate region close to the Si-SiO_2 interface (within few extrinsic Debye lengths) is avoided due to the interface proximity limitation [8]. An average value of N_a of about 10^{16} cm^{-3} is obtained which is consistent the value determined from the maximum-minimum high frequency C-V measurements performed on large area on-chip capacitors.

As discussed in Section III.4, The extracted values of C_{ox}, $C_B(V_g)$ and $C_{pn}(V_g, \omega)$ can be used to determine $C_{inv}(V_g)$ and consequently $C_{gc,p}(V_g)$ [eqn. (46)]. The obtained results of $C_{inv}(V_g)$ and $C_{gc,p}(V_g)$ are shown in Figures (4) and (6) respectively. In Figure (6), the extracted results, are compared to the measured high frequency (1 MHz) gate-channel capacitance. The significant deviation between the two characteristics, particularly near the onset of strong inversion, reflects the influence of interface traps in this region. Therefore, the use of the measured high frequency $C_{gc}(V_g)$ will lead to overestimated values for Q_{inv} and consequently, an underestimation of the effective channel mobility.

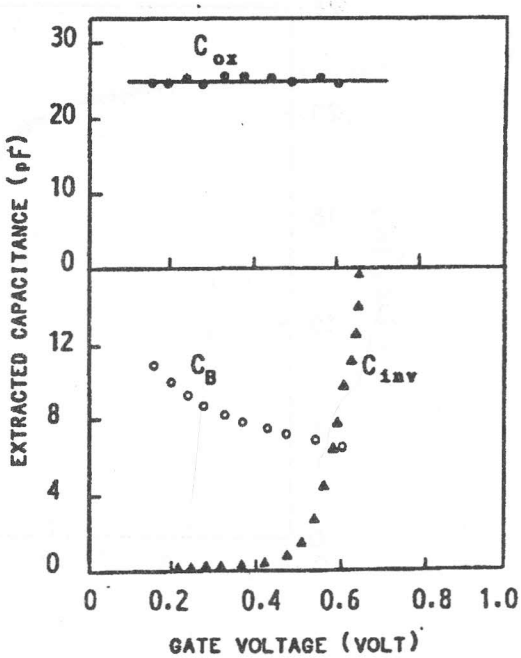

Figure 4. Extracted gate oxide capacitance C_{ox}, semiconductor bulk capacitance C_B and inversion layer capacitance C_{inv} as functions of gate bias using split-admittance measurements.

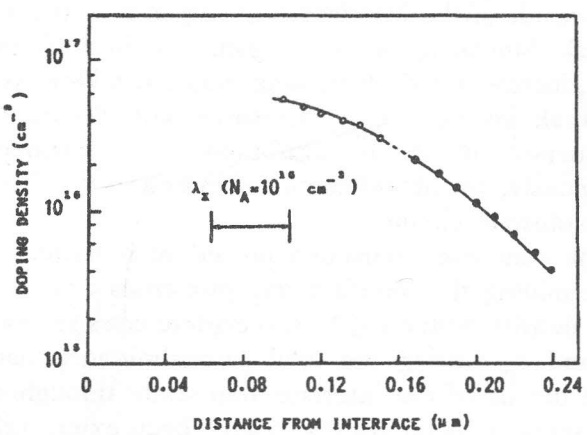

Figure 5. Extracted depth profile of the doping concentration as obtained using $C_B(V_g)$ results in weak inversion (filled circles) and using the high and low frequency $C_{gb,t}(V_g)$ data in depletion (empty circles).

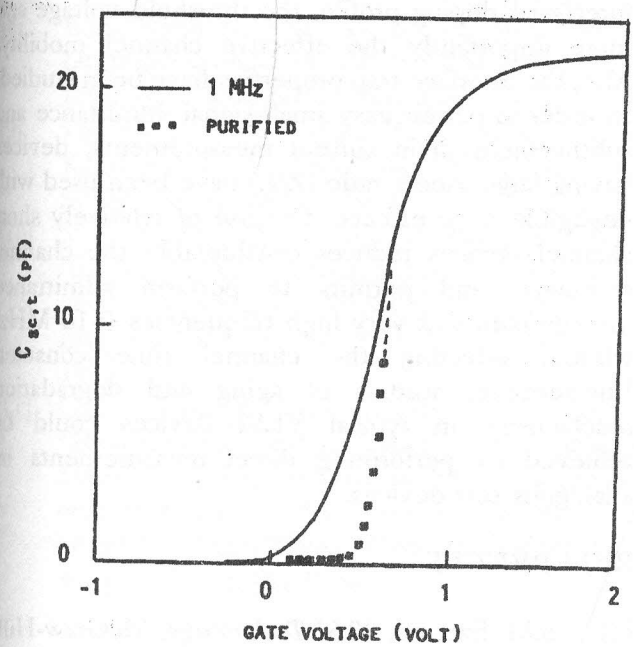

Figure 6. Comparison between the measured high frequency C_{gc} (solid line) measured at 1 MHz and the purified gate-channel capacitance $C_{gc,p}$ (squares) obtained using the split-admittance technique.

The evaluation of $\mu(V_g)$ is carried out using the extracted values of $Q_{inv}(V_g)$ and the transfer characteristics obtained at $V_d < kT/q$. Typical experimental I-V transfer characteristics are shown in Figure (7). The results are presented on linear and semi-log plots for different V_d values. The use of large aspect ratio devices enables noiseless current measurements even at very small gate bias ($V_g \sim 0.1V$). The semi-log plot exhibits a perfect linear behavior throughout the entire subthreshold region. Using the procedure discussed in Section III.4, $\mu(V_g)$ can be determined and the results are shown in Figure (8) for different drain biases. No mobility roll-off behavior has been observed in weak inversion even with relatively large values of V_d. However, significant difference between the $\mu(V_g)$ characteristics takes place when increasing V_d. This is expected since in weak inversion, I_d becomes independent of V_d when $V_d >> kT/q$. In this case, as seen from eqn (45), $\mu(V_g)$ becomes inversely proportional to V_d keeping in mind that $Q_{inv}(V_g)$ is determined from the split-admittance data at zero drain bias. As a result $\mu(V_g)$ decreases with increasing V_d. On the other hand, if one takes into account the dependence of Q_{inv} on V_d (particularly when $V_d >> kT/q$) the deviations between the $\mu(V_g, V_d)$ characteristics become insignificant. This is true since Q_{inv} decreases with increasing V_d which compensates the decrease in $\mu(V_g)$. This situation was studied extensively in Refs. [12] and [13] and accurate determination of $\mu(V_g)$ was performed using relatively large values of V_d. These values of V_d were needed to reduce the noise in the subthreshold drain current measurements since devices having unity aspect ratio (Z/L = 100/100) were used. In our case, a value of V_d as low as 10 mV, (significantly smaller than kT/q at room temperature), has been used to determine accurately $\mu(V_g)$, thanks to the large aspect ratio of the devices. For such low values of V_d, the assumption that Q_{inv} is not influenced by the drain bias seems quite reasonable.

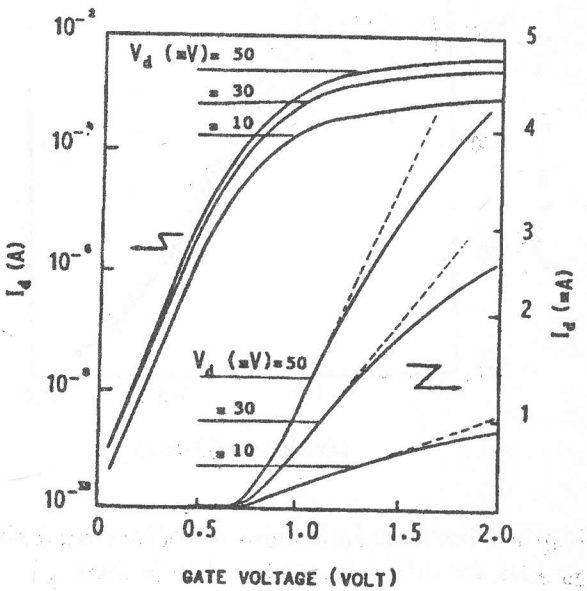

Figure 7. Typical transfer characteristics measured at different values of drain bias.

A final point to be discussed is the sensitivity and consequently the accuracy of the method. In fact, the accuracy with which the extracted device parameters are evaluated depends essentially on the sensitivity and accuracy of the split-admittance measurements. The best levels of accuracy are obtained using admittance bridges [8]. The sensitivity of these bridges is exploited most fully by

the conductance technique. With these bridges, interface trap densities in the 10^9 eV^{-1} cm^{-2} range near midgap can be measured. Devices having interface trap densities below 10^{10} eV^{-1} cm^{-2} are today's state of the art. Therefore, although the proposed technique is applied to devices having relatively high interface trap densities, the method is applicable to the state of the art devices as well. As mentioned previously, electrically stressed devices are studied to emphasize the capability of the method for accurate determination of device parameters in the presence of high interface trap densities.

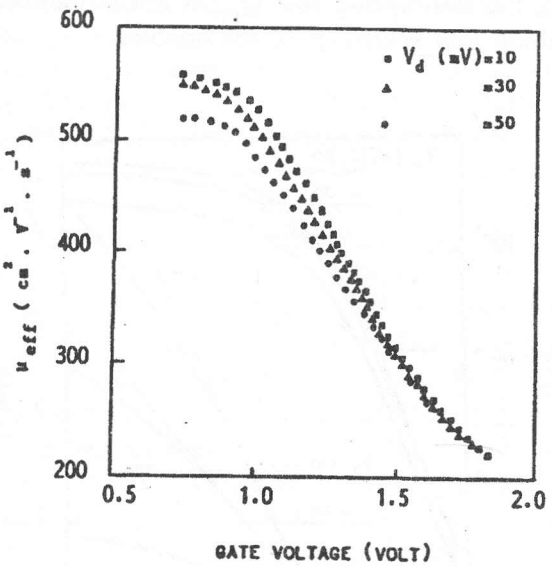

Figure 8. Extracted effective mobility curves versus gate bias for different values of drain bias.

VI. CONCLUSION

In this paper, a new analytical model for the split-admittances in short channel MOSFETs has been introduced. Based on this model, an experimental technique has been proposed for extracting device parameters by performing direct measurements on MOSFETs. The technique takes into consideration the effect of interface traps and allows accurate determination of several important parameters such as : the gate-oxide thickness, the interfacial doping profile, the threshold voltage and more importantly the effective channel mobility. Also, the interface trap properties have been studied. In order to permit easy small-signal admittance and subthreshold drain current measurements, devices having large aspect ratio (Z/L) have been used with negligible edge effects. The use of relatively short channel devices reduces considerably the channel resistance and permits to perform admittance measurements at very high frequencies (>10 MHz) without affecting the channel time constant. Furthermore, studies of aging and degradation mechanisms in typical VLSI devices could be achieved by performing direct measurements on analogous test devices.

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