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THE DESIGN OF AN ANALOG BY DIGITAL MULTIPLIER FOR ELECTROCARDIOGRAM SIGNAL PROCESSING

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ABSTRACT

An electronic circuit is designed for Electrocardiogram (ECG) signal-processing in which the ECG signal-in analog form- is multiplied by a digital factor (time independent).

The circuit is based on the idea of controlling the gain of an operational amplifier by a digital signal. The circuit is designed to multiply an ECG analog varying from -100 mV to +100 mV by a digital factor varying from -100 to + 100.

Experimental results show that for the specified input range the maximum error is 0.5 % and the multiplication is frequency indpendent up to 100 KHz.

INTRODUCTION

Several applications of microprocessors in ECG signal processing involves multiplication of the analog ECG signal by the microprocessor outputs which are usually digital numbers [1], [2]. There are the alternatives to perform this multiplication, namely to convert the digital number to an analog one and perform an anlog by analog multiplication, or to convert the analog ECG signal to a digital one and perform a digital by digital multiplication, or to perform a direct analog by digital multiplication.

The first two methods depend on the conversion of an analog signal to a digital one or vice versa. This makes the implementation of both circuits very complex and expensive. Also the conversion rate of the D/A or A/D limits the maximum input analog signal frequency. In our case, where real time multiplication is needed, very high speed D/A's or A/D's are required which makes the system even more complex and expensive. The conversion process itself, depending on the resolution of the D/A or A/D introduces errors that render inaccurate system.

As the third method does not involve any conversion, it is simpler, less expensive and more accurate. The aim of this work is to design a simple Analog by Digital Multiplier (ADM) to perform the multiplication of an analog signal by a digital factor in the real time and with convenient accuracy.

Concep of Multiplication

The concept of the analogy be digital multiplier (ADM) is based on the idea of controlling, by digital signal, the gain of an operational amplifier. Figure 1 shows the circuit of an operational amplifier as an inverting amplifier. The relation between the magnitudes of the output and input voltage signals is as follows:

$$V_o(t) = R_f/R_i * V_i(t) \qquad (1)$$

If we replace R_i by a set of parallel branches, each containing a resistance in series with a switch then the above relation becomes:

$$V_o(t) = R_f/R_t * V_i(t) \qquad (2)$$

where R_t is the parallel combination of the resistance of those branches whose switches are on. Each switch is controlled by a digital input bit such that it is closed when the input bit is at logical 1 and opened if it is at logical 0. The resistance R_b in series with each switch is chosen such that:

$$R_b = R/N \qquad (3)$$

where N is the weight of the digital input bit. For a 4-bit digital input word the circuit becomes as that shown in Figure 2.

Design of the Multiplier Basic Circuit

Consider the input digital word to be 8 bits wide, with the most significant bit reserved for the sign, the decimal equivalent of the digital input will vary from -128 to + 128, and the amplifier circuit of Figure 2 will be modified by introducing three more input branches. We assume the digital inputs to be TTL levels [3]. To implement the digitally controlled switches the CMOS Quad Bilateral switches (4066) [4] were used for the following features:

(i) Low On-resistance (270 ohms at VDD 0 + 5V)
(ii) Extremely low leakage current in the OFF state (0.1 nA).
(iii) Frequency response, switch on up to 40 MHz.
(iv) TTL compatability
(v) Low current switch controls
(vi) Analog signal range from (VSS-0.5) to (VDD + 0.5) volts
(vii) Low power consumption
(viii) Low price.

A schematic diagram of the 4066 switch package is shown in Figure 3.

The operational amplifier used in the circuit was chosen to be FET Dual operational amplifier (LF 353) for the following features:

(i) Wide gain bandwidth (40 MHz)
(ii) High input impedance (10^{12} ohms)

(iii) Low offset voltage (3 mV)

(iv) Low price.

A schematic diagram of the LF 353 package is shown in Fig 4.

The Most critical part of the circuit is the resistors. since the multilier accuracy depends upon the values of these resistances. The main factor determining the values of these resistances is the switch CN-resistance (R_{on} = 270 ohms). The smallest resistance in the parallel branches is the one corresponding to the most significant bit which equals to

$$R_6 = R/64 \tag{4}$$

Therefore for small error ,

$$R/\ 64 >> 270 \text{ ohms} \tag{5}$$

If we take R_6 to be 20 kilo-ohms, this gives sufficient accuracy. The values of the parallel resistors will thus be

$$\begin{aligned} R_o &= 1.28 \text{ mega-ohms} \\ R_1 &= 640 \text{ kilo-ohms} \\ R_2 &= 320 \text{ kilo-ohms} \\ R_3 &= 160 \text{ kilo-ohms} \\ R_4 &= 80 \text{ kilo-ohms} \\ R_5 &= 40 \text{ kilo-ohms} \\ R_6 &= 20 \text{ kilo-ohms} \end{aligned} \tag{6}$$

It is not easy to have this wide range of precision resistors. To overcome this, trimmers in series with fixed resistors are used to give a precise overall resistance.

The feedback resistor Rf should be equal to R, which is 1.28 mega-ohms, for correct multiplication. If we set the maximum analog input to be 100 mV and the maximum digital input to be $\pm$ 100, then the maximum output of the multiplier stage will be $\pm$ 10 V. But since the output of the multiplier stage is to drive the sign-bit stage, then Rf must be modified so as to bring down the maximum output of the multipler stage to the levels adequate for the sign-bit stage.

The circuit of Figure 5 is used to implement the sign-bit stage. It is such that when the sign-bit is at logical 0 then the digital word is taken to represent a positive number, and when the sign-bit is at logical 1 the number is a negative one. The output of the multiplier stage is fed to a 4066 switch. The input requirements of the switch is that the analog signal must be within VDD + 0.5 V and VSS - 0.5 V. Thus if Rf is halved, that is taken to be 640 kilo-ohms instead of 1.28 mega-ohms, then the output of the multiplier stage will be within $\pm$ 5 V.

For VDD = 5 V and VSS = - 5V this would be adequate since the 4066's input can thus vary from + 5.5 V to - 5.5 V.

An operational amplifier is used at the input to interface between the TTL digital input and the CMOS switch. The CMOS NOR Gate (4011) is used as an inverter. The final

operational amplifier was chosen to have a gain of 2 so as to compensate for the halving of Rf in the multiplier stage.

The final circuit of the analog by digital multiplier (ADM) is shown in Figure 6.

Experiments

The following experiments were made to check the accuracy resolution, and frequency response of the circuit: Experiment 1: The ADM was given a 100 mv input- the maximum design input-and the digital input was varied from 0 to 100 unit in steps of 1. The analog output was recorded.

Experiment 2: The ADM was given a sinusoidal input of 100 mV peak to peak and the digital input was set at 100. The frequency of the analog input signal was varied from d.c. to 1 MHz and the analog output was recorded.

RESULTS AND CONCLUSIONS

In experiment 1 an offset of 3 mV to 9 mV was observed. When the maximum offset, corresponding to digital input 0, was compensated for, the output had an error not exceeding 0.5 % as in Table 1.

Assuming that the digital input varies from -100 to +100 as stated earlier, the required resolution is (1/100) or 1 %. Thus the maximum allowable error is $\pm$ 0.5 %. From the

results of experiment 1 we can see that the circuit satisfies this condition.

Experiment 2 yielded that the output was constant for input analog frequencies from d.c. up to 100 KHz. This shows that our ADM is frequency-independent in this range.

The analog by digital multiplier (ADM) presented has the following advantages:

(i) Analog input level is between -100 mv and + 100 mv with a frequency spectrum up to 100 KHz.
(ii) Digital input is 8-bit in sign magnitude representation with a decimal equivalent range of -100 to + 100.
(iii) The output is analog and ranges between -10V and +10V.
(iv) The maximum error is 0.5% of the maximum output voltage.
(v) The multiplication is performed in the real time.

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Table 1 Results of experiment 1

Theor. o/p	Exp. o/p	Error%	Theor. o/p	Exp. o/p	Er
0	0.	0.	51	50.68	
1	0.98	0.02	52	51.67	
2	1.97	0.03	53	52.66	
3	2.96	0.04	54	53.64	
4	3.94	0.06	55	54.63	
5	4.93	0.07	56	55.60	
6	5.92	0.08	57	56.58	
7	6.91	0.08	58	57.57	
8	7.88	0.12	59	58.56	
9	8.85	0.14	60	59.55	
10	9.85	0.14	61	60.53	
11	10.84	0.16	62	61.52	
12	11.82	0.17	63	62.51	
13	12.81	0.21	64	64.17	
14	13.79	0.21	65	65.15	
15	14.78	0.21	66	66.14	
16	15.72	0.27	67	67.12	
17	16.71	0.28	68	68.11	
18	17.70	0.29	69	61.10	
19	18.68	0.31	70	70.09	
20	19.67	0.32	71	71.09	
21	20.60	0.33	72	72.04	
22	21.65	0.35	73	73.03	
23	22.64	0.39	74	74.02	
24	23.61	0.39	75	75.00	
25	24.60	0.42	76	75.99	
26	25.58	0.42	77	76.98	
27	26.57	0.42	78	77.96	
28	27.55	0.45	79	78.95	
29	28.54	0.46	80	79.99	
30	29.50	0.50	81	80.88	
31	30.51	0.49	82	81.85	
32	32.00	0.00	83	82.85	
33	32.98	0.02	84	83.83	
34	33.97	0.03	85	84.82	
35	34.95	0.04	86	85.81	
36	35.94	0.05	87	88.79	
37	36.94	0.06	88	87.76	
38	37.91	0.08	89	88.75	
39	38.90	0.09	90	89.74	
40	39.87	0.13	91	90.72	
41	40.86	0.14	92	91.71	
42	41.85	0.15	93	92.70	
43	42.83	0.17	94	93.68	
44	43.82	0.18	95	94.65	
45	44.81	0.18	96	96.15	
46	45.79	0.20	97	97.14	
47	46.78	0.21	98	98.12	
48	47.72	0.28	99	99.11	
49	48.71	0.28	100	100.10	
50	49.70	0.29			

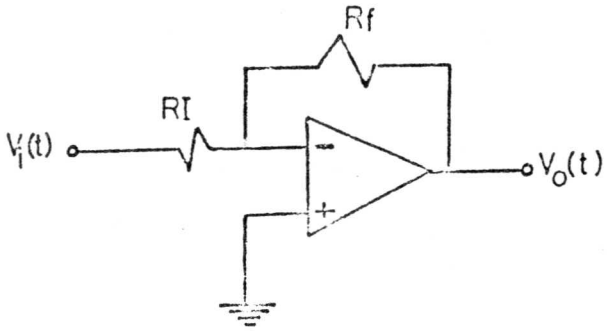

Figure 1

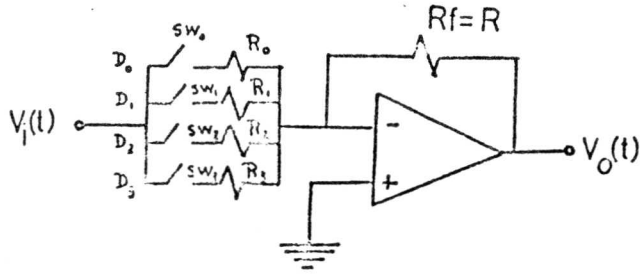

Figure 2

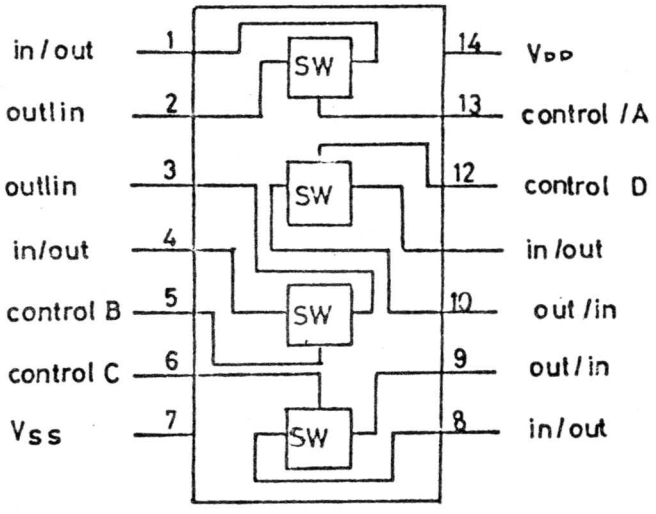

Figure 3

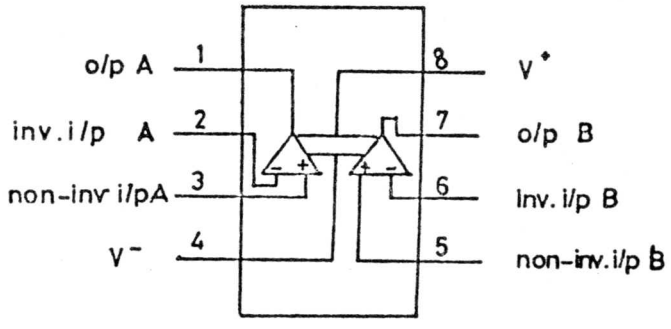

Figure 4

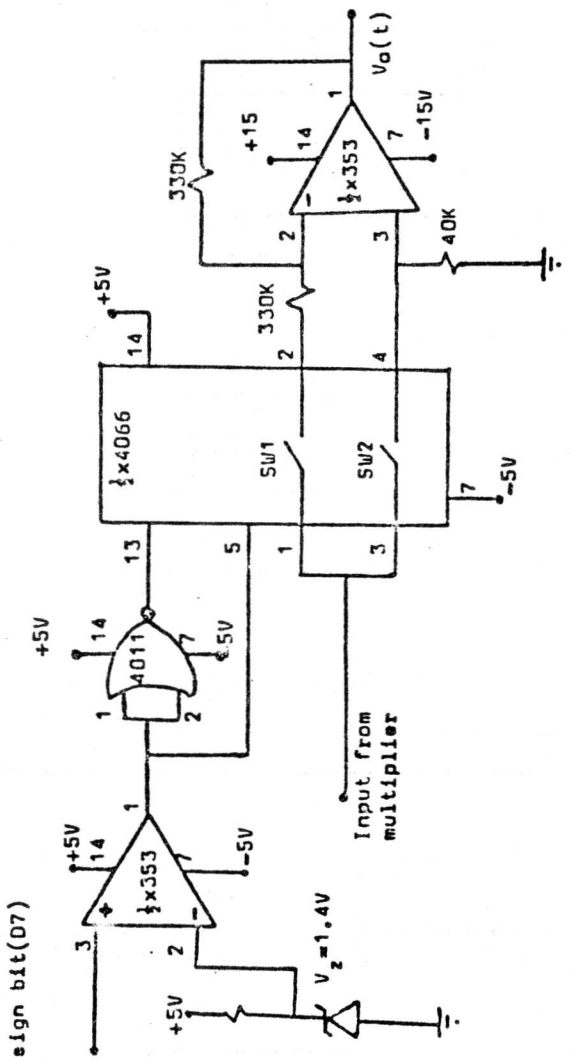
Vo(t)
+15
-15V
330K
40K
+5V
SW1
SW2
-5V
4066
4011
Input from multiplier
sign bit(D7)
Vz=1.4V

Figure 5

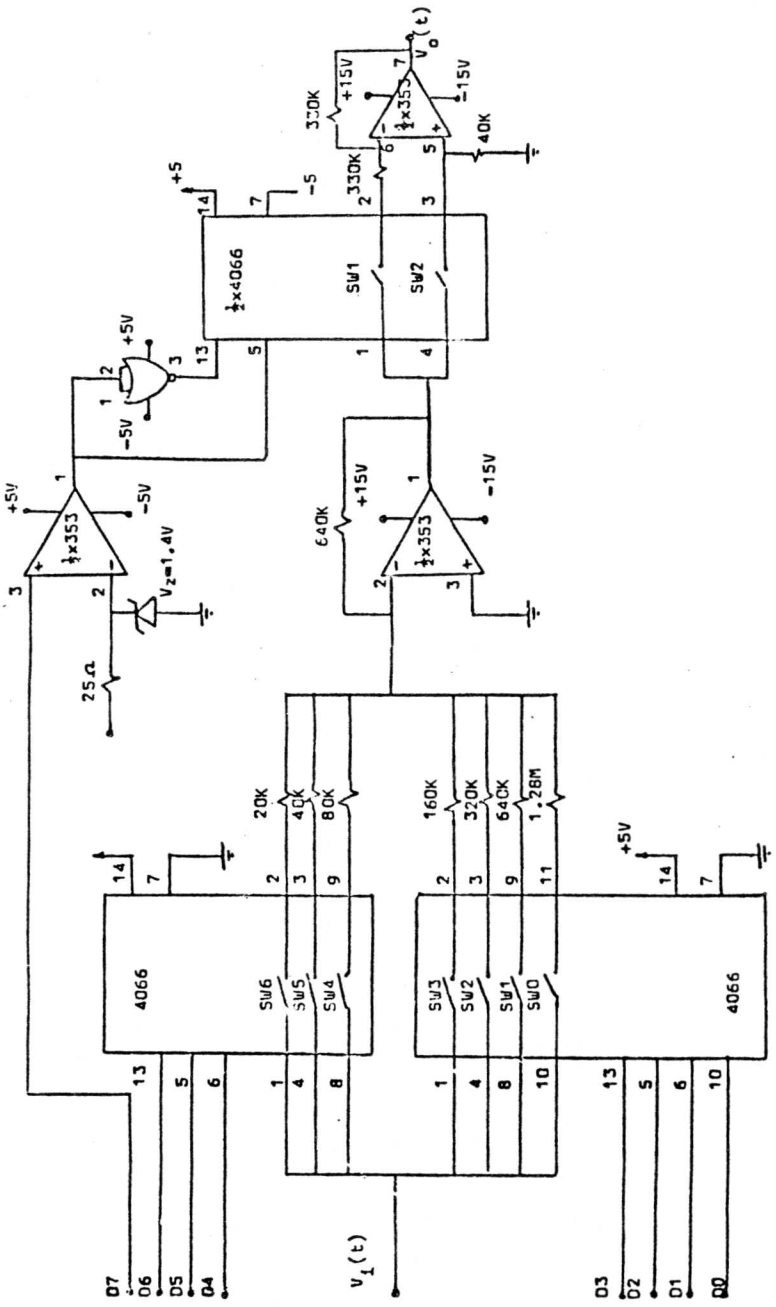
+15V
-15V
330K
40K
+5
-5
4x4066
SW1
SW2
+5V
-5V
4x353
V_2=1.4V
25Ω
640K
20K
40K
80K
160K
320K
640K
1.28M
4066
SW6
SW5
SW4
SW3
SW2
SW1
SW0
$V_o(t)$
$V_1(t)$
D7
D6
D5
D4
D3
D2
D1
D0

Figure 6