An analog VLSI cellular neuron

Mohamed El-Azab
Electronics and Communication Engg. Dept., Higher Technological Institute Ramadan Tenth, Cairo, Egypt

A cellular neural network with programmable parameters is proposed to recognize and classify the image patterns. It generates not only the ramp function but also its derivative. The neuron input signal is a current which is a sum of currents coming from a wideband CMOS transconductance synapses. The output driving current capability is sufficiently high for driving large capacitive loads. Activation of the two outputs can be conveniently controlled by means of mask programmable threshold voltage of Super MOSFET (SMOS) which has V_T as low as 100mV. The proposed circuit was implemented in a 0.34 µ m CMOS VLSI process and simulated by both Mat lab software and HSPICE to confirm the validity of the function. Comparing with the published [9-10] experimental results validate the proposed methodology.

يقدم هذا البحث شرحاً للخلية العصبية الاصطناعية والتى يقترح محاكاتها بخلية من الدوائر التكاملية متناهية الصغر وفى البحث محكاه للدوائر وتحديد لخواصها ومن المحاكاه تمكن من تحديد الخواص التى رأى أنها فى حدود المقبول.

Keywords: CMOS, Cellular neurons-Super MOS, Programmable parameters

1. Introduction

The Cellular Neural Networks (CNN) [1-10] are locally connected networks which can be implemented thanks to the advances in CMOS processes. The massive computational power, the low power consumption and the high level of intelligence of these networks make them ideally suited for real-time image processing, pattern recognition and other smart applications [11-15]. On the other hand, it is still a big challenge, where a lot of problems must be solved to achieve this goal. First, proper low power electronics must be worked out to realize basic operations required in the neural networks, second signals transmitted between neurons must be voltages, in order to avoid power losses in conductive paths. Since summation of currents is much easier to implement than summation of voltages, synapses should operate in a transconductance and neurons in an ohmic region. Moreover, information about the synapse weight should be stored within a chip, and analog memories seem to be adaquate for this purpose [16-18]. Various models of CMOS neurons have been developed and published [19-26]. The drawbacks attributed to analog VLSI, in general, are the limited available dynamic range and the channel length modulation effect through the early voltage.

In this paper we primarily focus on the major building blocks needed for a CMOS cellular neuron. Differential voltage current controlled source for making synaptic weights and a Super MOSFET, where the effect of the channel length modulation parameter is drastically reduced. Because of each neuron output needs to be sent to the other neurons, the output current needs to be repeated many times, this is accomplished by the bidirectional current mirrors. The block diagram of the proposed cellular neuron is shown in fig. 1, where the input is differential pair and the neuron has two outputs, the ramp r(t) and its derivative [27-30].

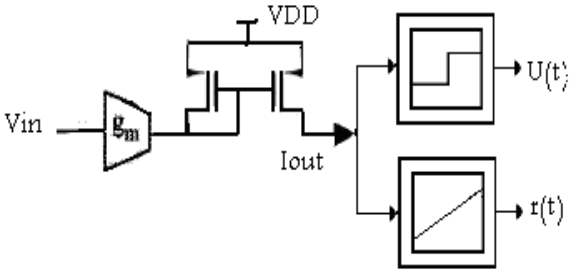


Fig. 1. Block diagram of the proposed CMOS neuron.

This paper is divided up into several sections. Section II presents the Circuit analysis, Circuit design is presented in section III, simulation results are discussed in section IV, section V presents a comparison with the published experimental results, and finally conclusion is presented in section VI.

2. Circuit analysis

The main function of the neuron may be summarized as follows: signals (action_potentials) appear at the unit's inputs (synapses). The effect of each signal may be approximated by multiplying the signal by some number or weight to indicate the strength of the synapse. The weighted signals are then summed to produce an overall activation. If this activation exceeds a certain threshold the unit produces the output response.

Fig. 2 represents the circuit diagram of a cellular neuron, whose output may be fed to the input of another neurons [18].

Straight forward analysis leads to the model of the neuron where the main function is to combine the input signals from other neurons, by summing weights. Bias current is usually added to shift values along the input axis. The activation function limits the amplitude of the output.

Then:

$$C_n \frac{dV_n}{dt} + G_n V_n = \sum_{n=1}^{n=N} g_{mn} R_n I_{in\,n} + I_{bias}, \quad (1)$$

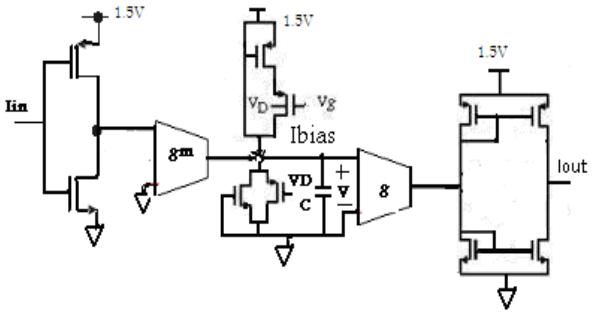


Fig. 2. Circuit diagram of the Cellular neuron.

where I_{in} is the input current to the neuron number n, R_n is the resistance represented by CMOS at the input of the synapse weight g_{mn}, I_{bias} is the bias current, V_n is the state variable action potential for activation, G_n is the conductance of the two MOS transistors that are connected in parallel and essentially function as a resistor and C_n is the smoothing capacitor which is Linear –Time Invariant (LTI) , for the nth neuron of a set N.[24-29].

2.1. A current mode sigmoidal function synapses circuit

Two of the key components in a cellular neuron are the weights and the nonlinear activation function. A weight can be realized by a tranceconductace operating in it is linear mode, while a sigmoidal non linear activation function can be obtained by operating a tranceconductace amplifier in its full nonlinear range. Fig. 3. Shows the current mode sigmoidal circuit.

Simplified circuit analysis shows the linear dependence of the output current on the square-root of the bias current [22].

$$I_{out} = V_{in} \sqrt{K I_{bias}} \quad . \quad (2)$$

Where I_{out} is the output current and V_{in} is the difference between the two inputs V_{in1} and V_{in2}, I_{bias} is the bias current and K is a constant. The transconductance G of the amplifier was the slope of the output current against the input voltage curve:

$$G = \frac{I_{out}}{V_{in}} = \sqrt{K I_{bias}} \quad . \quad (3)$$

It is noticed that the dependence of bandwidth and tranceconductance on the bias current indicates the possibility of control on the performance through varying the bias current.

2.2. A programable current mode sigmoidal model

Transistors SN and SP are super MOS [24] and are connected in parallel and essentially function as a resistor as shown in fig. 3.

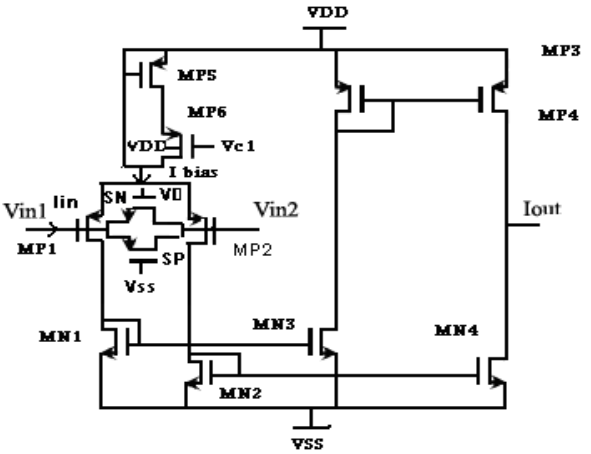


Fig. 3. Acurrent – mode sigmoidal circuit.

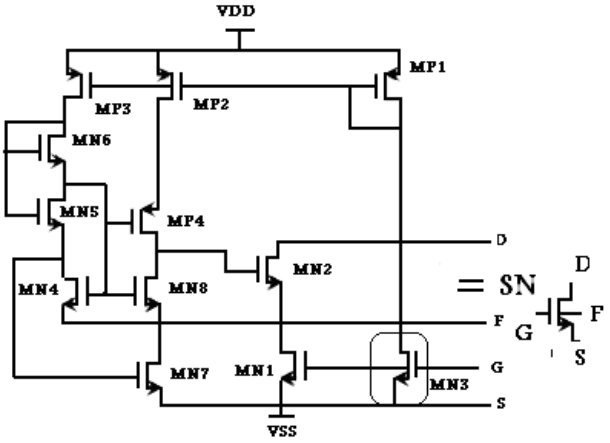


Fig. 4. N-type Super MOS (SN).

Therefore, we have the transconductance obtained as:

$$g_m = \frac{k}{2}(V_{DD} + V_{TP} - V_{TN}), \quad (4)$$

where k is the transconductance parameter, V_{TP} and V_{TN} are the threshold voltage of SP and SN respectively. We note that:

$$V_{in} = \frac{I_{in}}{g_m}. \quad (5)$$

Then the output current will be:

$$I_{out} = \frac{I_{in}}{g_m}\sqrt{K I_{bias}}. \quad (6)$$

To get the relation between threshold voltage of the super MOS and the channel width (W_3) of the transistor MN3 shown in fig. 4, we assume that all transistors are working in saturation region. Then for MN3 the drain current will be:

$$I_D = K\frac{W}{2L}(V_{GS} - V_T)^2, \quad (7)$$

where L is the channel length and W is the channel width, then

$$V_{GS3} = V_{TN} + \sqrt{\frac{2I_{D3}L_3}{KW_3}}. \quad (8)$$

As V_T = 0.75 V then we have:

$$V_{TN} = K_1 - \frac{K_2}{\sqrt{W_3}}, \quad (9)$$

where K_1 and K_2 are constants.

From eqs. (4, 6 and 9) one can obtain:

$$I_{out} = \frac{I_{in}}{(V_{DD} - \frac{K^{\backslash}}{\sqrt{W_3}} + \frac{K^{\backslash\backslash}}{\sqrt{W_3}})}\sqrt{K I_{bias}}, \quad (10)$$

where W_3 is the cannel width of MOSFET MN3 , $K^{\backslash}$ and $K^{\backslash\backslash}$ are the constants of the Super MOS –SN, that show the feasibility of mask programming for the threshold voltage which can reach as low as 100 mV. This is obtained by varying only the channel width (ω_3) of one transistor in the SMOS architecture.

3. Circuit design

In order to avoid power losses in conductive paths, synapses should operate in a transconductance and neurons in an ohmic mode. More over, information about the synapse weight should be stored within analog

memories. An improved version of the neuron circuit is proposed. The improvement relies on adding a second output at which the voltage is linearly dependent on the neuron input current. In this way, we obtain a neuron with two outputs, i.e. a step-function output and a linear one. Fig. 5 presents the proposed Cellular neuron circuit [30-34]

The trnsconductance synapses is a device that generates at its output a current that is a function of the difference between two input voltages, as shown in fig. 3. The two transistors MP5 and MP6 are used as a current source, its drain voltage is large enough that the drain current I_{bias} is saturated at a value set by the gate voltage V_{c1}. The three current mirrors MN1, MN5 and MN2, MN4 besides MP3, MP4 are used to generate an output current that is proportional to the difference between the two differential drain currents. The current drawn out of MP1 is reflected as an equal current of MP4 and the current drawn out of MP2 is reflected as equal current out of MN4. Transistors SN and SP are Super MOS and are connected in parallel and essentially function as a resistor [22].

As shown in fig. 4. Super MOS behaves like a cascade MOS transistor having source, gate and drain terminal., but with nearly zero channel modulation factor (λ) and intrinsic gain "gmro" of more than 90dB. The super MOS however has an extremely high output impedance due to implementation of the gain boosting technique. Also, the effect of the channel length modulation parameter (λ) on the output current of MOSFE is drastically reduced in SMOS which means that the SMOS may be used in a perfect matched current mirror [24].

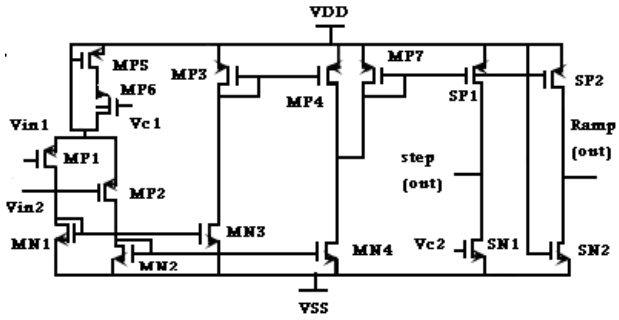


Fig. 5. The proposed Cellular neuron circuit.

Referring to fig. 5, at the step output, each transistors SN1 and SP1 can operate either in saturation or in Ohmic region, depending on the control voltage V_{c2} and the input current coming from synapses. Where V_{c2} is gate to source voltage, that controls the operation of SN1. The active state of the neuron occurred if the input current is higher than the drain current, the output voltage V_{out1} is then approximately equal V_{DD}. On the other hand, if the input current is less than the drain current, SP1 is in saturation and SN1 is forced to operate in the Ohmic region, which is an inactive state of the neuron and V_{out} is close to zero.

The second ramp output could be realized as follows: the transistor SN2 works in the Ohmic region and leads SP2 transistor. An operation in this region takes place when drain to source voltage VDS, gate to source voltage VGS and the threshold voltage V_T of SP2 fullfill the following relation:

$$V_{DS} \prec (V_{GS} - V_{TP}). \quad (11)$$

As ($V_{GS} - V_{TP}$) is higher, the more linear is the transistor channel resistance. As a result, the ramp (out) voltage is approximately proportionally to the drain current. A channel resistance, required to operate with low currents is obtained for a long and narrow channel of SP2 [35-42]

4. Simulation results

Results presented in this section concern a 0.18 μm CMOS process. The neuron properties as well as its cooperation with synapses were simulated. Other properties of the transcondutance synapses and the super MOSFET have been descried in [22-24]. Layout of the simulated circuits was made using Mentor Graphics and simulations performed by means of HSPICE and PSPICE.. Parasitic elements resulting from the layout have been taken into account in electrical schems of the circuits examined. Threshold voltages of the SMOS N-type and P-type transistors were equal to 100mV, -100mV. In fig. 6, the synapses output current as a function of the difference voltage is shown.

Fig. 7, shows the transfer characteristics concerning the step output of the neuron. DC properties at the output of the neuron was investigated. Fig. 8 shows Simulated Time response of the neuron step output.

Comparing with the published Measured [9-10]. The neuron with linear output have been investigated. Speed and stability of the neuron operation, for the case of V_T = 200mV, is illustrated in fig. 9. The activation function which is similar to the sigmoid can be obtained as shown in fig. 10.

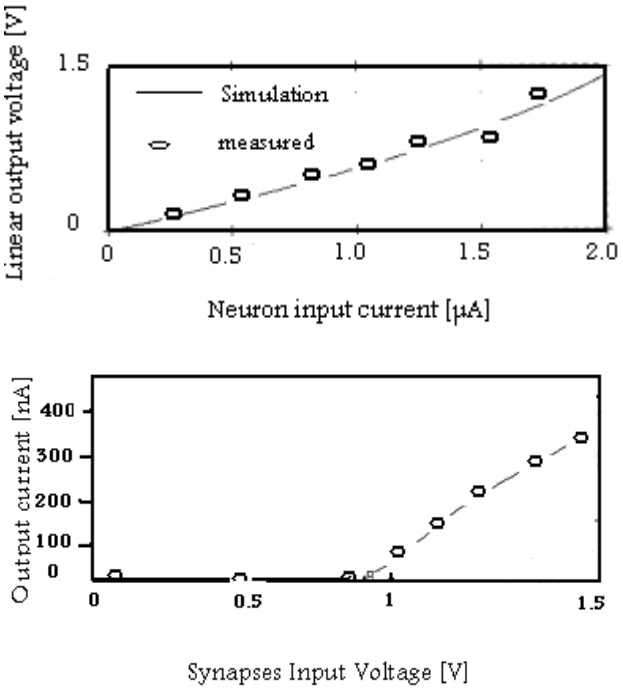


Fig. 6. Simulated synapses output current against the difference input voltage.

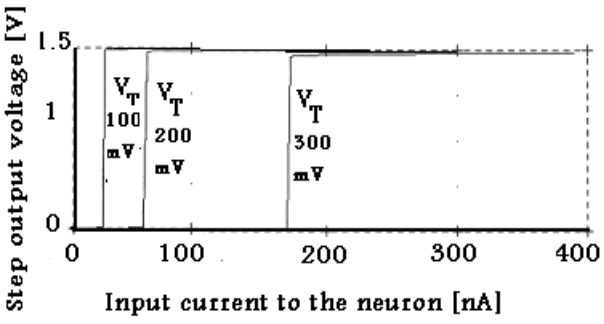
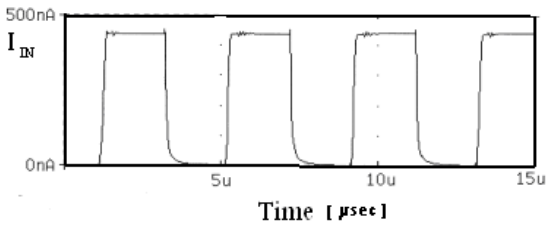


Fig. 7. Simulated transfer characteristic of the step output neuron.



Time response at the neuron step output

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Fig. 8. Simulated Time response of the neuron step output.

Fig. 9. The measured [9-10] and Simulated linear output voltage of the neuron versus its input current.

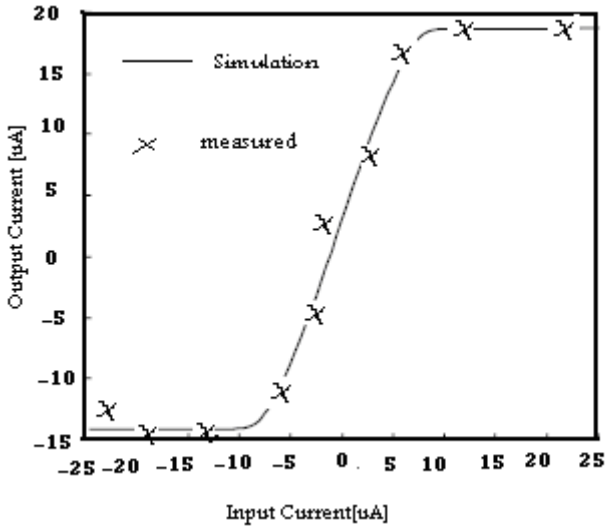

Fig. 10. Measured [9-10] and simulated Activation function of the cellular neuron circuit.

6. Conclusion

Analog VLSI cellular neuron with programmable parameters has transconductance synapses and two output neuron was presented and analyzed. All the circuits are confirmed by HSPICE simulation using 0.18μm CMOS technology. The proposed circuit has many advantages over the simple transconductance. The obtained bandwidth reaches 400 MHz which is suitable for wide band operation cellular neuron. The output driving current capability is sufficiently high for driving large capacitive loads. The super MOS whose threshold voltage is mask

programmable through changing the dimensions of a single MOS. In general, programmable and modular artificial neural networks can be built using the proposed circuits.

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