Wideband CMOS-LC voltage controlled oscillators with low-phase-noise

Mohamed Alazab
Higher technological Institute, Department of Electronics and Computer Eng. Ramadan Tength, Egypt
Ingo@hdf.org.eg

A CMOS-LC Voltage controlled Oscillator (VCO) has been designed and simulated using a simulation-based genetic optimization tool called AMIGO. This VCO achieves a 25 % tuning range with a control voltage ranging from 0-3.3V and loads to a 2.4GHz fully integrated oscillator using 0.35-μmCMOS technology. On-chip spirals are used in place of resistors to provide a low noise bias point to the varactors. The On-chip spirals achieve more than1.17nH of effective inductance while consuming a die area of 300×300 μm^2. The simulated single –ended phase noise is – 106 dBc/Hz at 600 KHz offset from a 2.4GHz carrier when the VCO core is drawing 4.77mA from a 3.3 V supply.

يقدم هذا البحث نموذج لمذبذب ذو ترددات عالية جدا ويتم التحكم فى التردد بواسطة الجهد والذى يستخدم فى دوائر التحكم المغلقة. والتكنولوجيا المستخدمة بواسطة نموذج م.و.س. مما يضمن ضوضاء قليلة ورقم معايرة مقبول. ولقد تمت محاكاة الدائرة المقترحة والنتائج جيدة.

Keywords: Voltage Controlled Oscillator (VCO), CMOS technology, Differential Voltage Current Controlled Source (DVCCS)

1. Introduction

Voltage Controlled Oscillator (VCO) is an essential building blocks of modern wireless communication systems. Its performance in terms of tuning range, phase noise, and power dissipation determines many of basic performance characteristics of a transceiver. The VCO is widely utilized as clocking source in all kinds of transceivers. With growing in demands in broadband data access to internet, carrier frequency for Wireless Local Area Networks (WLAN) and Bluetooth technology has been pushed beyond 2.4GHz. In each of these applications, the low cost provided by fully integrated CMOS solution is very attractive. In spite of relaxation oscillators easily achieve very wide tuning range (i.e. 100% or more), their poor phase noise performance is the main drawback [1].

CMOS LC-VCO is a superior candidate to achieve low noise for the inherent band pass filtering of LC resonator that can suppress side-band noise. It has allowed for full integration of precise analog filters. The LC VCO is called Harmonic Oscillator because it is capable of produce an almost pure sinusoidal oscillation with good phase noise which represents the phase and frequency fluctuations and spectral purity. It is modeled as a negative resistance oscillator where the tank circuit determines the frequency while the active circuit is called energy restorer [2].

On the other hand, VCO is an integral part of the Phase Locked Loop (PLL), clock recovery circuits, and frequency synthesizers. Random fluctuations in the output frequency of the VCO expressed in terms of jitter and phase noise , have a direct impact on the signal-to nose ratio where frequency translation is performed. In particular, RF oscillators employed in wireless transceivers must meet certain phase noise requirements, typically mandating the use of passive LC tanks with a high quality factor (*Q*). However, the trend towards large-scale integration low cost makes it desirable to implement oscillators monolithically [3].

Recently, several wideband CMOS LC VCO's have been demonstrated using a variety of techniques. The high intrinsic Cmax / Cmin of inversion-or accumulation – type MOS varactors supports a very wide tuning range and their Q is sufficiently high that good phase noise performance can be determined [4].

In this paper, fully differential voltage current - controlled source followed by current mirror as a turbo charger to fully differential VCO are proposed. This technique has benefit of guaranteed start up and well controlled amplitude beside low phase noise and reasonable figure of merit.

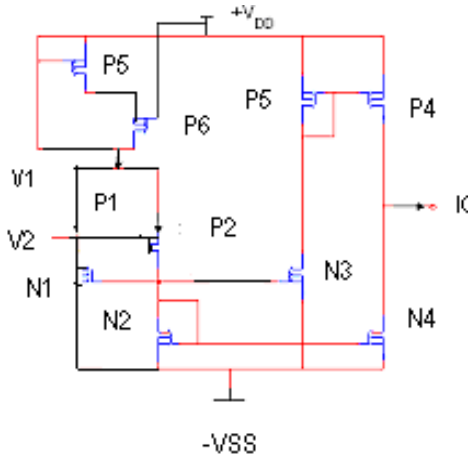
The basic concept of the proposed circuit is given in section II, In section III phase noise modeling is presented and simulation results are presented in section IV. Finally conclusions are given in section IV.

2. Basic concept of the proposed circuit

2.1. Differential Voltage Current Controlled Source (DVCCS)

The DVCCS is a device that generates as its output a current is a function of the difference between two input voltages, The differential pair is shown in fig. 1 as an input stage P1 and P2. The two transistors P5 and P6 are used as a current source, under normal circumstances; its drain voltage is large enough that the drain current Ibias is saturated at a value set by the gate voltage Vg. The manner in which Ibias is divided between P1 and P2 is a sensitive function of the difference between V1 and V2 and is the essence of the operation of the stage. The three current mirrors N1, and N3, N2, N4 beside P3, P4 are used to generate an output current that is proportional to difference between the two differential drain currents 11 and 12. where the current 11 drawn out of P1 is reflected as an equal current out of P4 and the current 12 drawn out of P2 is reflected as equal current out of N4.

To implement this function we design the circuit in 0.35µm COMS technology. All transistors work in the saturation mode for the specified output current level. The design procedure starts by adjusting the DC potential level at the gate of the bias current source P6 and at the outputs at half the supply voltage with both inputs shorted to ground. The transfer characteristics are then obtained using ideal (I-V) converter at the output terminal. The linear range is obviously the range of interest which should be extended in range and improved in linearity [5].



[P1, P2, N2, N3, N4, P3, P4 (8/034)]
[P5, P6 (12/0.34)] [N1 (21/034)]

Fig. 1. The Differential Voltage Current Controlled Source (DVCCS).

Simplified current analysis shows the dependence of the DVCCS transeconductance *Gm* on the square root of the bias current:

$$G_m = \frac{I_{out}}{V_{in}} = \sqrt{K\, I_{bais}}\,. \tag{1}$$

$$K = \mu \frac{W}{L}\, C_{ox}\,. \tag{2}$$

Where

(L/W) is the aspect ratio of the MOSFET which is a design parameter,

M is the electron effective mobility in the Channel, and

C_{ox} is the gate oxide capacitance per unit area.

2.2. CMOS LC-VCO

The VCO used in this paper is the complementary cross coupled oscillator shown in fig. 2 , which consists of P1, P2, N1, N2, L1, L2 and a two MOSFET capacitors, Cb1 Cb2 are employed for switched –band coarse tuning.. The PMOS current source which has good phase noise response with respect to the one uses a NMOS pair and where the 1/f noise of PMOS is generally found be less than for an NMOS with the same dimensions [6].

The conductance Gm of the tank circuit is:

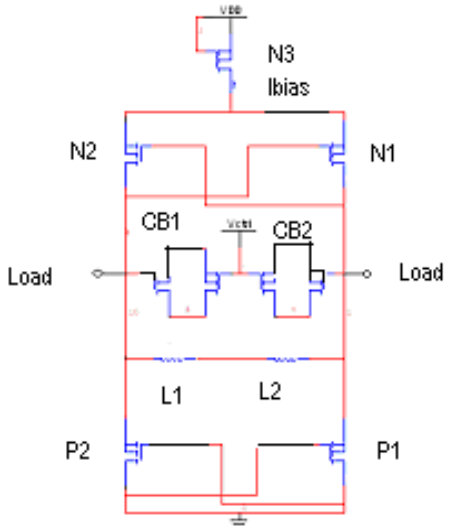


Fig. 2. The LC-VCO circuit diagram.

$$G_m = \frac{1}{2}[G_L + G_{VARACTOR} + G_{ds,n} + G_{ds,p}]. \quad (3)$$

Where G_L represent the conductance associated with the coil, $G_{Varacter}$ is the Transeconductance of the varactor, and $G_{ds,n}$, $G_{ds,p}$ are the transeconductance of NMOS and PMOS respectively.

The tank filters the non sinusoidal current signal coming from the energy restorer of the two cross coupled transistor , they have gate of one transistor connected to the drain of the other and vice versa and its sources short circuited. The conductance seen from the drain of the two cross.–coupled transistor block is negative. Assuming that the transistor's in saturation then the equivalent capacitance seen by the drains of the transistors is.

$$C_{eq} = 2C_{gd} + \frac{1}{2}[C_{gs} + C_{db} + C_{ds} + C_{gb}] \ . \quad (4)$$

The main requirement for VCO design are that tuning range must cover the entire band of operation, phase noise should be minimized at the oscillation frequency, signal power must be high enough to provide the load and circuit power consumption.

In our design these requirements are satisfied since:

The cross coupled transistors: work as a negative resistance that sustains oscillation by compensating loss in the LC tank and frequency is controlled by varying the capacitance of the tank The on-chip spiral inductor is simulated with EM (Electro-Magnetic) simulator ASITIC. The quality factor (Q) can be improved by increasing metal width.

The tranceconductance Gm of the cress-coupled MOS pairs must be high enough to compensate the loss of the tank. The length of the transistor, must be reduce in order to minimize parasitic sources of loss measured by the quality of L (QL) and quality of C (Qc) and the output impedance *Gm* must be larger than the total loss.

Phase noise is uncertainty of center frequency of VCO output, where the spectrum looks as if it has finite power in certain frequency offset away from the center frequency. In time domain phase noise is referred to as timing jitter [7].

Detailed circuit schematic of CMOS LC–VCO is shown in fig. 3, which considering the cross coupled block model and parasitic of the varactor and inductor ….

3.2. Phase noise model and VCO performance

Despite the oscillator is itself a non linear system because its signal amplitude is limited, the relation between the noise and excess phase can be reasonably assumed to be linear if it is considered that the imposed perturbations are small compared to the main oscillation

Consider an LC lossy tank at which an impulse current is injected when the signal is a maximum, only the amplitude modified, but if it is injected at zero-crossing times, only the phase changes. At other times, both amplitude and phase change. Then, depending on the time the injection occurs is the disturbance in the phase, which means that the system is Linear Time Variant (LTV) system. A current impulse at the input of the tank generates a change in the charge of the tank capacitor *C* without change in the inductor current. The excess phase $\Phi(t)$ generated by a current unit impulse can be calculated as follows [8].

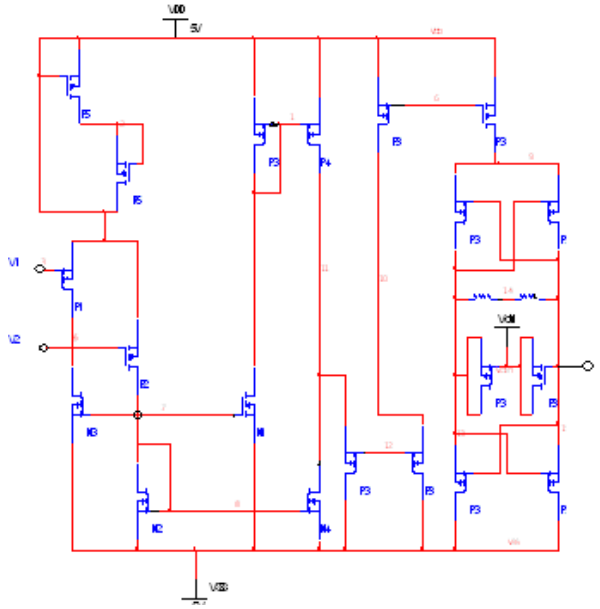


Fig. 3.The proposed CMOS LC-VCO circuit diagram.

The current source

$$i(t) = I_{\max} \sin(m\omega_o + \Delta\omega), \tag{5}$$

where

$$\Delta\omega \prec \omega_o \ , \tag{6}$$

and m = 1, 2, 3,...

The convolution ϕ(t) of the impulse response of the current in the band $\pm\Delta\omega$, can be calculated as follows:

$$\phi(t) = \int_{-\infty}^{+\infty} h(\tau)\, i(t-\tau)dt \ , \tag{7}$$

where $h(\tau)$ is the impulse response of the tank circuit and $i(t-\tau)$ is the current impulse.

If C_m is the Fourier series coefficient and q_{max} is the maximum charge of the capacitor, the phase noise is [9]:

$$\phi(t) = \frac{I_{\max} C_m \sin(\Delta\omega)}{2q_{\max}\Delta\omega}. \tag{8}$$

$$\phi(t) = \frac{I_{\max}}{2q_{\max}} C_m \ \operatorname{sinc} \ \Delta\omega, \tag{9}$$

which means that the phase –noise is two sided energy signal. The VCO performance can be compared by means of a Figure Of Merit (FOM), as defined in [1]. A figure of merit is presented as means of comparing different VCO's techniques.

$$VCO_{FOM} = \phi(t)\ dBc/Hz - 20\log\frac{f_{osc}}{f_{offset}} + 10\log\frac{P_{diss}}{1mw}, \tag{10}$$

where f_{osc} is the carrier frequency, , foffest is the frequency offset, Pdiss is the power consumed by the VCO core, and ϕ (t) is the phase noise simulated at an offset foffest from the carrier.

The simulated phase noise is -106 dBc/ Hz at 100 kHz, offset was achieved at an output frequency of (2.73 GHz) draws (9mA) from (3.3V) and supply (29.7mW), which gives a figure of merit of -180.7dBc/Hz.

3. Simulation results

We have designed the DVCCS. SPICE has been used to carry out the different types of analysis which gives a transfer function characteristics with given bias current The tranceconductance slope is about 160µs.

On the other hand, we have also used an optimizer called Analog Migration for IC's based on Genetic Optimization (AMIGO). The results obtained from AMIGO represent the best values of the variables that satisfy all design constraints [10], including the cross-coupled transistor sizes, the bias transistor size, and the bias voltage that maintains the bias transistor in saturation. The used transistors are divided into fingers of maximum width imposed by the technology. The accumulation-mode MOS varactor provides low power consumption and low phase noise. The oscillator tuning range is found to be 25%. After optimization, simulation is performed again offline using ELDO RFIC to verify and characterize the performance of the VCO. All results meet the performance specifications initially imposed. The simulated phase noise at 600 HZ offset from 2.4 GHz carrier is given in fig. 4 and the frequency response is shown if fig. 5.

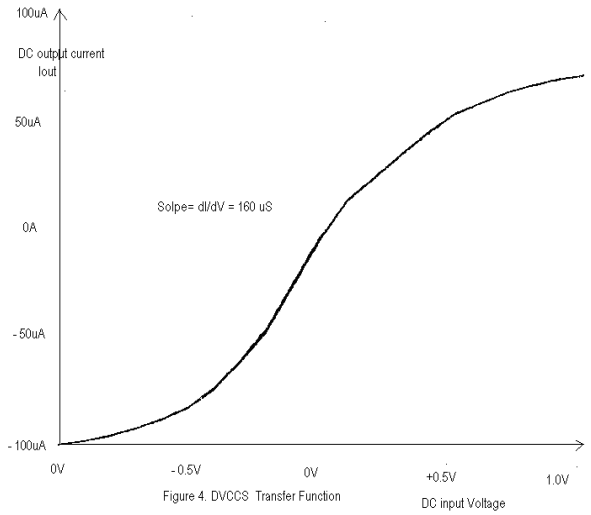


Figure 4. DVCCS Transfer Function

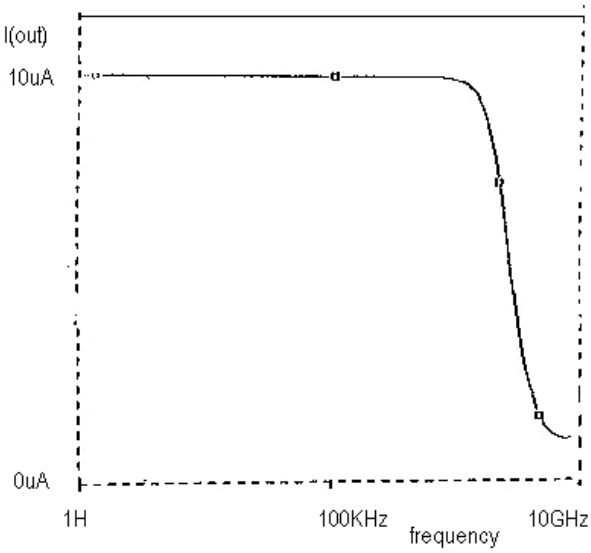


Fig. 5. DVCCS frequency response.

Table 1
Amigo results

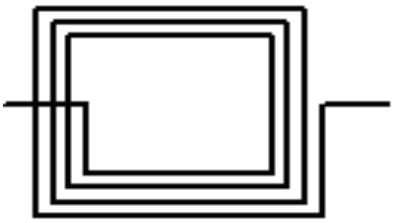
Variables	Value
P MOS_W	310µ /11 fingers
N MOS_W	220µ/11 fingers
QL	6@2.2 GHz
Qc	16.8 - 58.7 @2.4GHz

The selected passive elements (on-chip) spiral coil and it equivalent circuit taken from the standard 0.35-um CMOS SPICE models is shown in fig. 6.

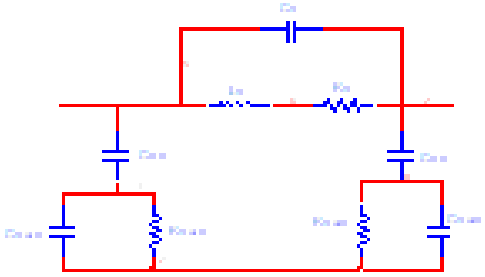
The layout of the accumulation – mode MOS varactor is composed of a number of parallel connected small capacitors. It is made up of rows in vertical direction, and columns in horizontal direction. The total width of the varactor is calculated to be equal to (Row*Col* width of a segment). The width of a segment is fixed and equal to 6.6µm [10].

4. Conclusions

New proposed turbo charger VCO has been described. The circuit is guaranteed to start oscillation and provide well- controlled amplitude. The circuit has been simulated and all aspects of its performance havebeen confirmed. Comparison with published work for the same oscillator topology show that our design reasonably competes with other work [11], specially for the tuning range.



(a) Physical layout



(b) Equivalent circuit of spiral inductor

Fig. 6. Spiral coil and its equivalent circuit.

Table 2
VCO performace comparison

	Ham [1]	This work
Tech. (µm)	0.35	0.35
Cener frequency	2.33 GHz	2.4 GHz
Ibias	4mA	4.77mA
Phase -noise	-115 dBc/Hz	-107 dBc/Hz
FOM dBc/Hz	175dBc/Hz	180.7dBc/Hz
Tuning range	26%	25%
Power consumption	10mW	15.74mW

Acknowledgment

This work is supported by ICL –Ain Shams University and Mentor Graphic-Egypt. The authors would like to thank Professor Hani Fikry and Prof Adel El-Henawey for their excellent advices.

References

[1] D. Harn and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LCVCOs", IEEEJ. Solid-state Giants, Vol. 36, pp. 896-909, June (2001).

[2] M. Zannoth, B. Kolb, J. Fenk and R. Weigel, "A Fully Inte Grated VCO at 2 GHz," IEEE J. Solid-State Giants, Vol. 33, pp. 1987- 1991, Dec. (1998).

[3] C. Larn and B. Razavi, "A2,6-GHz/5,2 GHz CMOS Voltage-Controlled Oscillator", in ISSCC Dig. Tech, Papers, pp. 402-403 (1999).

[4] M. Hers He Nson, A. Hajimiri, S.S. Mohan, S.P. Boyd and T.H. Lee, "Design and Optimization of LC Oscillators", in Proc., IEEE/ ACM Int. Conf Computer Aided Design, San Jose, CA, pp. 65 – 69, Now (1999).

[5] M. Alazab, "Design and Simulation of a Wideband CMOS Transcondutance Amplifier", In Proc., URISI, NRSC'99, D6.

[6] Warren. David A.J. Michael Golio and L. Seely, "Large and Small Signal Oscillator Analysis", Microwave Journal, Vol. 32 (5), pp. 229-246, May (1989).

[7] A. Hajimiri and T.H Lee, "Design Issues in CMOS Differential LC Oscillators", IEEE J. Solid – State Giants, Vol. 34, pp. 717-724, May (1999).

[8] H. Wang. A Hajimiri and T.H. Lee, "Come Spondence: Comments on Design Issues in CMOS Differential LC Oscillators", IEEE ?J, Solid-State Circnts, Vol. 35, pp. 286-287, Feb (2000).

[9] C. De Ranter, G. Van Der Plas, M. Steyaert, G. Gielen and W. Sansen, "Cyclone: Automated Design and Layout of RFLC- Oscillator", IEEE Trans. on Computer- Aide d Design of Integrated Circuits and Systems, Vol. 21, pp. 1161-1170, Oct. (2002).

[10] S. Abd El-Khalik, S. Kayed, M.A. Al Azab, M. Dessouky and H.F. Ragai, "Automated Synthesis of Integrated RF CMOS LC VCOs", International Conference on Electrical, Electronic and Computer Engineering (2004).

[11] S.M. Abdel-Khalik "Design Automation of LC Ocillators", Msc. Thesis, Ain Shams University, Egypt (2004).

Received June 5, 2007
Accepted November 11, 2007