Voltage stability analysis in multi-infeed HVDC systems

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The far more complicated dynamics of the multi-infeed type HVDC systems arise mainly from the interactions of multi-infeed converters and the simultaneous operation of a variety of controls to achieve voltage stability. In this paper, a novel analysis of voltage stability in Multi-Infeed HVDC systems is carried out. The dynamics of the entire integrated system pre, during and post contingencies are thoroughly considered. The effect of different corrective actions such as control mode choice and reactive power enhancement on the AC-DC system stability is studied at different short circuit ratios.

ترجع تعقيدات التغيرات الديناميكيه فى نظم التيار المستمر متعددة الأطراف أساسا إلى التأثير المتبادل للموحدات إضافة إلى الإحتياج لتشغيل العديد من المتحكمات لتحقيق إستقرار الجهد. و تقدم هذه الورقه البحثيه طريقه جديده لتحليل إستقرار الجهد فى نظم الجهد الفائق المستمر متعددة الأطراف. و قد تم أخذ التغيرات الديناميكيه لكامل النظام قبل و أثناء و بعد الحالات الطارئة فى الإعتبار. كما تمت دراسة تأثير الإجراءات التصحيحية مثل تغيير نوع التحكم أو تدعيم القدرة الغير فعالة على إستقرار النظام عند مختلف نسب القصر.

Keywords: MIF, HVDC, Voltage stability

1. Introduction

In recent years, as the use of HVDC transmission continues to develop, situations increased where HVDC links terminate in close proximity in a common AC system area. Such configurations, known as multi-infeed or multi-terminal HVDC systems, are already apparent in various locations all over the world. Several researchers analyzed voltage instability problems in single-infeed HVDC systems from a static prospective [1-4], other researchers developed these techniques to be suitable for multi-infeed HVDC systems [5, 6]. Furthermore, a lot of work dealt with voltage instability as a dynamic phenomenon for single-infeed HVDC systems [7-11]. Nevertheless, relatively fewer research works dealt with dynamic instability of multi-infeed HVDC systems [7, 12-14].

D. Lee and G. Anderson [7], presented the principles of dynamic voltage instability of multi-infeed HVDC system considering the DC line as simple RL circuit with a current or power controller in its rectifier side and a fixed extinction angle control in its inverter side. Nayak et al. [13] presented the interaction effects between different HVDC lines in multi-infeed systems. X.F. Yuan [14], presented the dynamic simulation of Multi-InFeed HVDC system (MIF) with sudden disturbance with only one control mode of operation.

Zhao and Sun [15] studied the effect of nonlinear Voltage Source Converter (VSC) control on multi-infeed dc system stability. Their model utilized the reactive compensating effect of the VSC.

In this paper, the analysis of voltage instability in a more detailed Multi-Infeed HVDC system (MIF) has been carried out considering the dynamics of the DC system and DC system controllers using the Eigenvalues analysis and the system response to short circuit ratio variations. The system's performance under all possible control modes groups was simulated. The results were compared with that of static analysis. The improvement of stability is carried out using DC system parameters and by transferring to other DC system control modes. Furthermore, SVC is used to help overcome this problem. The results of small signal stability model are validated using nonlinear simulation.
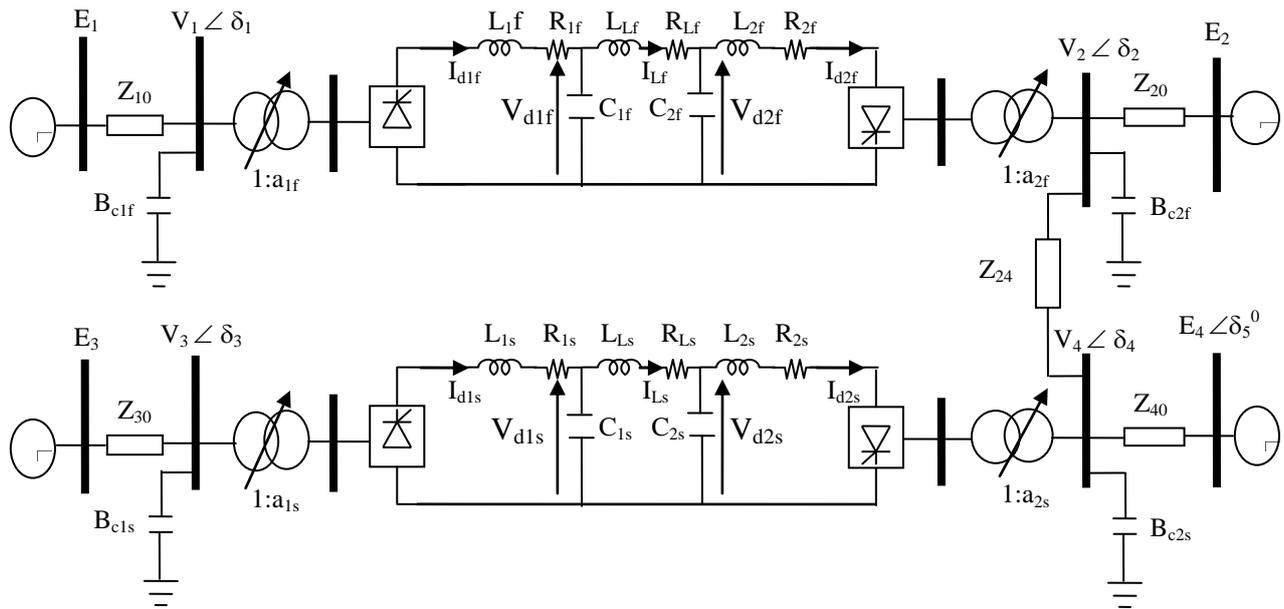
Fig. 1. Multi Infeed HVDC transmission system.

2. System model

2.1. System configurations

A general MIF system is shown in fig. 1. The AC system was represented by its Thevenin's equivalent at fundamental frequency viewed from the converter bus. The DC transmission lines are represented by their π-equivalent circuits. E_1, E_2 and E_3 are considered as reference for AC isolated regions 1, 2 and 3. The power flows between isolated regions are maintained by DC system controllers.

2.2. Model of DC system and controllers

The DC system consists of converters, controllers, smoothing reactors and DC lines. The DC networks shown in fig. 1 are represented by the following equations, where ''j'' denotes ''f'' for the first network, and ''s'' for the second one:

$$\dot{I}_{d1j} = (E_{O1j} - R_{C1j}I_{d1j} - V_{d1j})/L_{1j} \quad . \tag{1}$$

$$\dot{V}_{d1j} = (I_{d1j} - I_{Lj})/C_{1j} \quad . \tag{2}$$

$$\dot{V}_{d2j} = (I_{Lj} - I_{d2j})/C_{2j} \quad . \tag{3}$$

$$\dot{I}_{Lj} = (V_{d1j} - R_{Lj}I_{Lj} - V_{d1j})/L_{Lj} \quad . \tag{4}$$

$$\dot{I}_{d2j} = (V_{d2j} - R_{C2j}I_{d2j} - E_{O2j})/L_{2j} \quad . \tag{5}$$

Where

$$E_{O1f} = k_{1f}a_{1j}V_1 \cos\alpha_f \ .$$

$$E_{O2i} = k_{2f}a_{2f}V_2 \cos\beta_f \ .$$

$$E_{O1s} = k_{1s}a_{1s}V_3 \cos\alpha_s \ .$$

$$E_{O2s} = k_{2s}a_{2s}V_4 \cos\beta_s \ .$$

As $(\alpha, \beta)_{f,s}$ are Rectifier delay angle and inverter advance angle of first and second DC lines respectively.

The DC system controller consists of either a current, power, voltage or constant delay angle controller at rectifier side.

The inverter controller consists of either a current, power, voltage, constant extinction angle or constant advance angle controller. The current/power controller at the jth terminal is shown in fig. 2.

The differential equations of a Proportional - Integral (PI) current controller at rectifier side of first DC line can be written as follows [1, 3]:
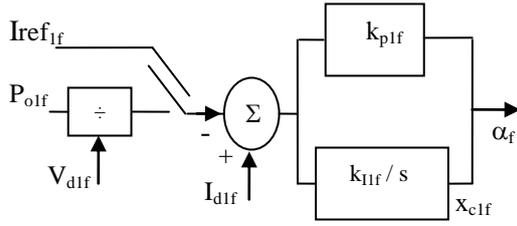
Fig. 2. Constant current / power controller
for rectifier side.

$$\dot{x}_{c1f} = k_{If}(I_{d1f} - I_{ref_{1f}}), \tag{6}$$

$$\alpha_f = x_{c1f} + k_{P1f}(I_{d1f} - I_{ref_{1f}}), \tag{7}$$

where:

k_{If}, k_{Pf} are the integral and proportional current controller gain of first DC line respectively, and

$x_{c1f,}$ is the output of integral controller branch.

Eqs. (6 and 7) are replaced according to the applied type of controller. For a power controller, eqs. (6 and 7) are replaced by:

$$I_{o1f} = \frac{p_{o1f}}{V_{d1f}}, \tag{8}$$

$$\dot{x}_{c1f} = k_{If}(I_{d1f} - I_{o1f}). \tag{9}$$

$$\alpha_f = x_{c1f} + k_{P1f}(I_{d1f} - I_{o1f}). \tag{10}$$

The constant DC voltage controller is similar to the current controller except for the input being the DC voltage and its reference value.

3. AC-DC power flow model

The system power flow algebraic equations at converter buses can be written as follows [16-17]:

$$g_{Pi} = V_i[\,V_iY_{ii}\cos\theta_{ii} + Y_{i0}E_i\cos(\theta_{i0} - \delta_i)$$
$$+ \sum_{j=1}^{j=5} V_jY_{ij}\cos(\theta_{ij} + \delta_j - \delta_i)] \pm P_{dnm} = 0, \tag{11}$$

$$g_{Qi} = -V_i[\,V_iY_{ii}\sin\theta_{ii} + Y_{i0}E_i\sin(\theta_{i0} - \delta_i)$$
$$+ \sum_{j=1}^{j=5} V_jY_{ij}\sin(\theta_{ij} + \delta_j - \delta_i)] + Q_{dnm} - Q_{sj} = 0. \tag{12}$$

Where

$$P_{dnm} = V_{dnm}\ I_{dnm}\ .$$

$$Q_{dnm} = V_{dnm}\ I_{dnm}\ \tan\ \phi_{nm}\ .$$

$$\cos\ \phi_{nm} = \cos\ \alpha_{nm} - (R_{Cnm}\ I_{dnm})/(k_{nm}\ a_{nm}\ V_i)\ .$$

$$\bar{Y}_{ii} = \sum_{j=1}^{j=5} 1/\bar{Z}_{ij} + jB_{Ci} = Y_{ii}\angle\theta_{ii},\ i = 1,2,....5$$

$$\bar{Y}_{ij} = -1/\bar{Z}_{ij} = Y_{ij}\angle\theta_{ij},,\ i = 1,2,....,5,\ j \neq i\ .$$

$$\bar{Y}_{i0} = -1/\bar{Z}_{i0} = Y_{i0}\angle\theta_{i0},,\ i = 1,2,3,4\ .$$

$$n = 1,2 \qquad m = f,s\ .$$

Q_{Sj} is the reactive power injected at ith AC bus,

P_{dnm}, Q_{dnm} are the rectifiers and inverters DC active and reactive power respectively,

$\cos, \Phi_{nm}$ are the rectifiers and inverters power factors, and

K_{nm}, k_{nm} are the rectifiers and inverters constants.

4. Mathematical model of overall system

The system's differential equations can be linearized to obtain the state space model [5]:

$$\dot{x}_{DC} = A\ x_{DC} + B\ u_{DC}\ . \tag{13}$$

Where
x_{DC}, u_{DC} are the mismatch of system state variables and DC system inputs

$$x^t_{DC} = [\Delta x_{c1f}, \Delta x_{c2f}, \Delta I_{d1f}, \Delta I_{d2f}, \Delta V_{d1f}, \Delta V_{d2f}, \Delta I_{L1f},$$
$$\Delta x_{c1s}, \Delta x_{c2s}, \Delta I_{d1s}, \Delta I_{d2s}, \Delta V_{d1s}, \Delta V_{d2s}, \Delta I_{L1s}]$$

$$u^t_{DC} = [\Delta\delta_1, \Delta\delta_2, \Delta\delta_3, \Delta\delta_4, \Delta\delta_5, \Delta V_1,$$
$$\Delta V_2, \Delta V_3, \Delta V_4]$$

By linearizing the system algebraic eqs. (11 and 12), the state space form of algebraic equations is obtained:

$$0 = C x_{DC} + D u_{DC} \quad . \tag{14}$$

Where "C", and "D" are the Jacobian submatrices.

Assuming that D remains nonsingular along system trajectories as the system parameters vary, then eqs. (13 and 14) are reduced to:

$$\dot{x}_{DC} = A' x_{DC} \quad . \tag{15}$$

Where

$$A' = A - B D^{-1} C \quad .$$

Eq. (15) represents the small signal stability model of the Differential Algebraic Equations (DAE) suitable for MIF system. Voltage stability analysis is carried out by computing Eigenvalues of system state matrix A'.

The Voltage Sensitivity (stability) Factor (*VSF*) is calculated from the relation for a general form HVDC as follows:

$$u_{DC} = [VSF] \Delta Q_s \quad . \tag{16}$$

where

$$\Delta Q_s = [Q_{s1} \ Q_{s2} \ Q_{s3} \ Q_{s4}]$$

$$[VSF] = (-C A^{-1} B + D)^{-1} G \quad . \tag{17}$$

where

$$G = \frac{\partial g}{\partial Q_s} \quad \text{and} \quad g^t = [g_{Pi}, g_{Qi}]$$

Where $VSF_{(i,j)}$ is the partial derivative of the ith converter bus voltage w.r.t. reactive power supply at the jth converter bus.

5. Case study

The multi-infeed system is still relatively under research and more complex to analyze [13]. The system's performance and dynamic behavior are still considered to be related to the same items describing the behavior of single-infeed HVDC systems. Nevertheless, additions aspects are needed to be considered due to the presence of other converters nearby. Under such disturbances, the effects are transferred from the DC systems though the interconnected AC lines which generate the dynamic interactions between the converters. The interactions effect is evident in the modeled system results under different DC system control modes. The AC system strength is measured by the short circuit ratio defined by $SCR_i = 1/Z_i$, "i" is the converter bus number.

The data of the MIF system used to implement the proposed technique is given in appendix 1.

Fig. 3 shows the change of line voltages at both rectifier and inverter buses as a function of SCR_{Invs}. The line voltage at inverter side of second DC line is found to be more sensitive to the decrease of SCR compared with that of other AC buses. The system power flow failed to obtain solution at SCR_{Invs} of 1.70765 as the adopted control mode boundary was reached. The phase shifts at AC buses versus SCR_{Invs} are also shown. The increase of phase shift at inverter bus of second DC line with SCR decrease is greater than that at other AC buses. The decrease of line voltage and phase angles is consistent and demonstrates the expected deterioration of stability at low SCR values.

Fig. 4 corresponds to a stable case (SCR_{Rects} = 2.5994), The rectifier is on CDA control while the inverter is on CC control for both of the two DC lines.

Fig. 4-a shows that a small change occurs in the inverter current due to CC in inverter side while a large change occurs in rectifier side current which reaches steady state after 0.1 sec.

Fig. 4-b shows that a small change occurs in both of the rectifier and inverter currents due to a small change in AC bus of first DC line. This illustrates the interaction effect between the two DC lines.

Fig 4-c shows the phase plane of AC line voltage versus DC line current at the rectifier and inverter side of second DC line. The figure illustrates that both AC voltages reach a stable node point.
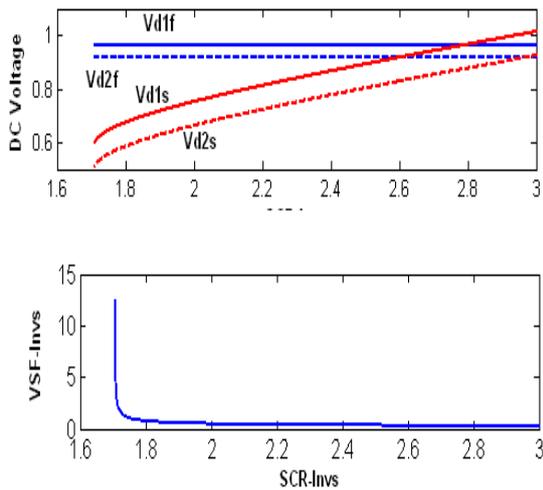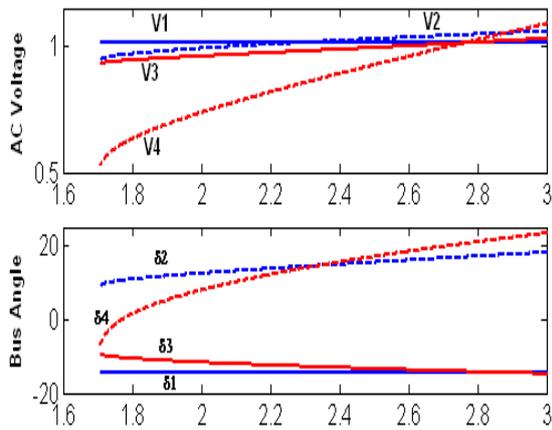
Fig. 3. System variables versus SCR$_{\text{Invs}}$. (1$^{\text{st}}$ DC line adopts CDV/CC and 2$^{\text{nd}}$ adopts CC/Cβ).
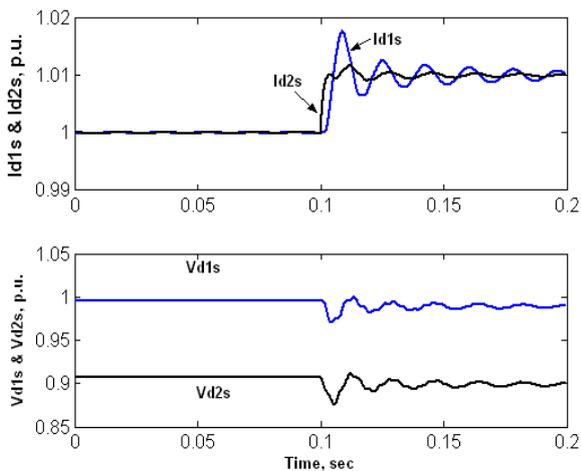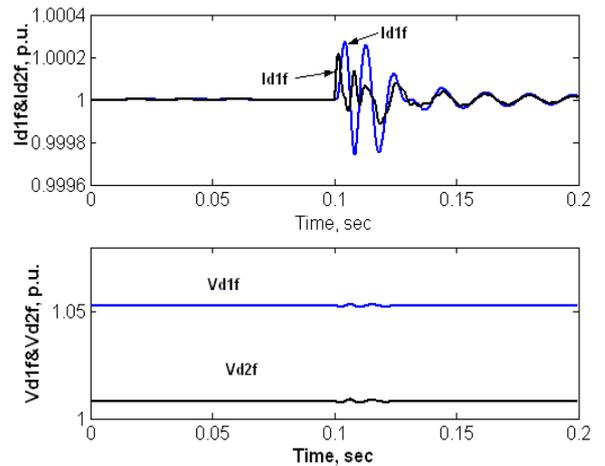

Fig. 4-a. Time responses of second DC line.

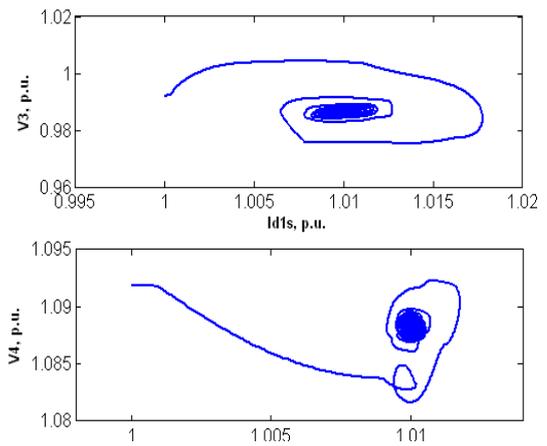Fig. 4-b. Time responses of first DC line.

Fig. 4-c. Phase plane of V$_3$, I$_{\text{d1s}}$, V$_4$ and I$_{\text{d2s}}$

Fig. 4. Effect of 0.01 step in 2$^{\text{nd}}$ line's current order (both lines on CDA/CC).

Figs. 5-a, 5b and 5c correspond to a stable case (SCR$_{\text{Rectf}}$ = 1.57555). The first DC line operates at CDA/CC control mode while the second DC line operates at CC/Cβ control. Fig. 5-a shows the time response of DC line current at both rectifier and inverter of first DC line to a step increase in rectifier current order by 0.001 p.u. A small change will occur in inverter current due to CC in inverter side while a large change occurs in rectifier side current which reaches steady state after 0.15 sec.

Fig. 5-b shows the time response of AC line voltage and phase shift at inverter of first DC line at a small increase in rectifier current order by 0.001 p.u. Both reach steady state

after 0.15 second from current order mismatch. Fig5-c shows the phase plane of AC line voltage at the rectifier and inverter side of first DC line versus DC line current. The figure illustrates that both AC voltages reach a stable node point.

Fig. 6 corresponds to an unstable case; SCR_{Rects}=1.8702 (Saddle Node Bifurcation). The rectifier is on CDA control while the inverter is on CC control for both DC lines. Fig. 6-a shows the time response of DC line current at both rectifier and inverter first line. A small change occurs in inverter current due to CC controller in inverter side while a large change occurs in rectifier current corresponding to a transition away from a stable point. Fig. 6-b shows the phase plane of AC line voltage of first DC line against DC line current. The response illustrates the transition from stable to unstable points.

The instability limits of the different adopted control modes are illustrated in table 1 in trms of short circuit ratios at rectifier and / or inverter stations, where SN and PF stand for "Saddle Node Bifurcations" and "Power Flow Failed" respectively.

6. Stability improvement

Several techniques are applied to improve system stability. This paper discusses the effect of control mode selection and / or static reactive VAR compensation at converter bus on voltage stability.
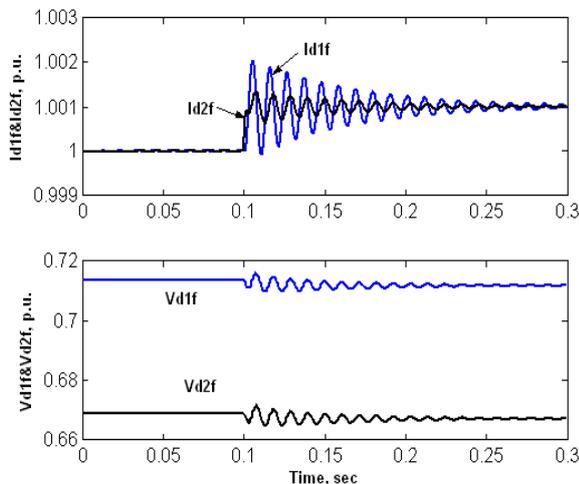

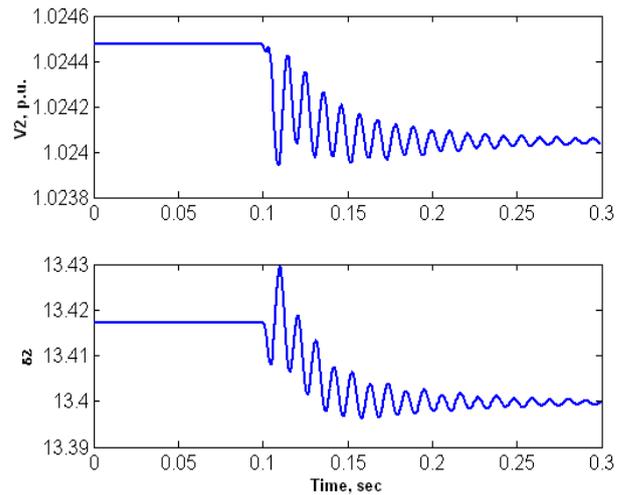Fig. 5-a. Time responses of DC line current and voltage of the first DC line.

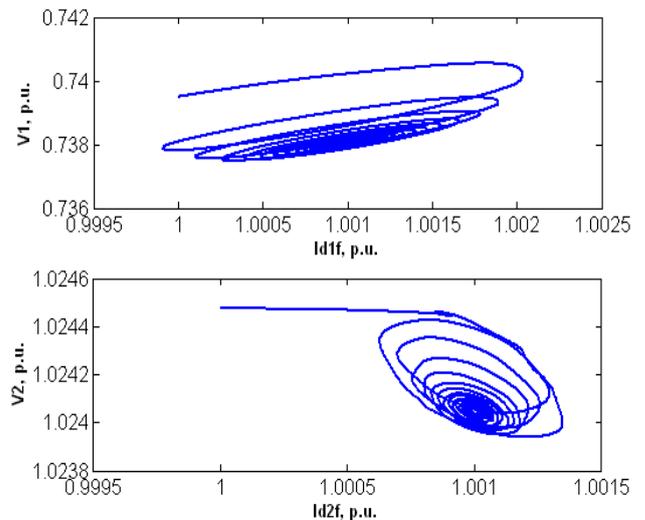Fig. 5-b. Time response of AC line voltage and Phase shift at inverter of first DC line.

Fig. 5-c. Phase plane of V_1 , I_{d1f} , V_2 and I_{d2f}.

Fig. 5. Effect of 0.001 step increase in 2nd line's current order (1st line on CDA/CC, and 2nd line on CC/Cβ).

Furthermore, the reactive power effect attained by installing shunt capacitors in the DC line sides was also assessed.

6.1. Installing DC line shunt capacitance

Fig. 7 shows the effect of adding 0.06 sec. (p.u.) capacitor at rectifier of second DC line at SCR_{Rects} of 1.8702 (SN point). A relatively large time was needed to loose stability as shown.

Such delayed instability allows application of other corrective actions adequately.

Installing the 0.06 sec. (p.u.) capacitor at the inverter bus of the second DC line instead of the rectifier side converted the Saddle Node point to a stable case. The system variables reached steady state after about 0.4 sec.

6.2. Change of control mode

Fig. 8 shows the effect of transferring the second DC line from CDA/CP to CDA/CC control mode on DC line current and voltage of second DC line which illustrates that the system reached steady state after 0.1 second instead of loosing its stability.

6.3. Applying a static VAR compensator

The dynamic model of a Static VAR Compensator SVC is taken as a proportional voltage regulator, a simplified model of SVC is given by [5] as:

$$\frac{\partial Q_{svc}}{\partial t} = \frac{[k_{svc}(U_{ref} - U_j)U_j^2 - Q_{svc})]}{T_{svc}} \quad . \quad (18)$$

where: k_{svc}, T_{svc}, U_{Ref} and Q_{svc} are the proportional gain, controller time constant, voltage setpoint and static var compensator reactive power. The system's differential equations are modified by adding eq. (18) and the algebraic equations are also modified by inclusion of the SVC reactive output power Q_{svc}.

Table 1
System Instability for different modes

| Control modes	SCR
CDA/CC and CDA/CC	SCR_{Rectf} 1.939112 (SN), SCR_{Rects} 1.939112 (SN)
CDA/CC and CDA/CP	SCR_{Rectf} 1.939112 (SN), SCR_{Rects} 3.090175 (PF)
CDA/CC and CC/Cβ	SCR_{Rectf} 1.939112 (SN), SCR_{Invs} 2.449180 (PF)
CDA/CC and CDV/CC	SCR_{Rectf} 1.939112 (SN), SCR_{Rects} 2.633658 (PF)
CC/Cβ and CDA/CC	SCR_{Invf} -2.30787 (PF), SCR_{Rects} 1.942125 (PF)
CP/Cβ and CDV/CC	SCR_{Invf} -2.28676 (PF), SCR_{Rects} 2.144542 (PF)
CC/Cβ and CDA/CP	SCR_{Invf} -2.051282 (PF), SCR_{Rects} 2.763194 (SN)
CDV/CC and CC/Cβ	SCR_{Rectf} 2.313744 (PF), SCR_{Invs} 1.707650 (PF)
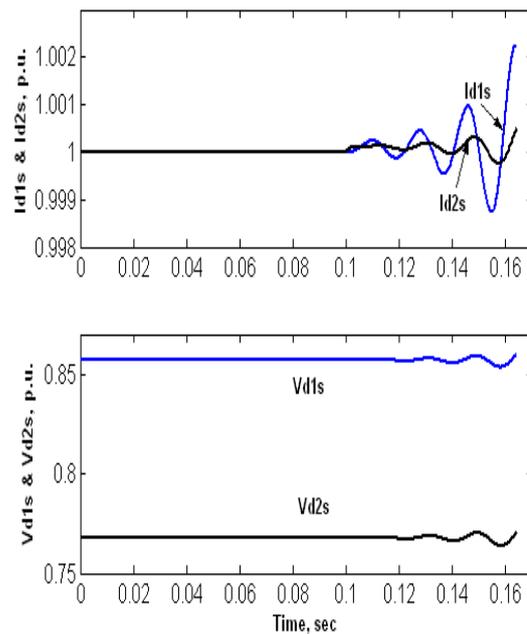
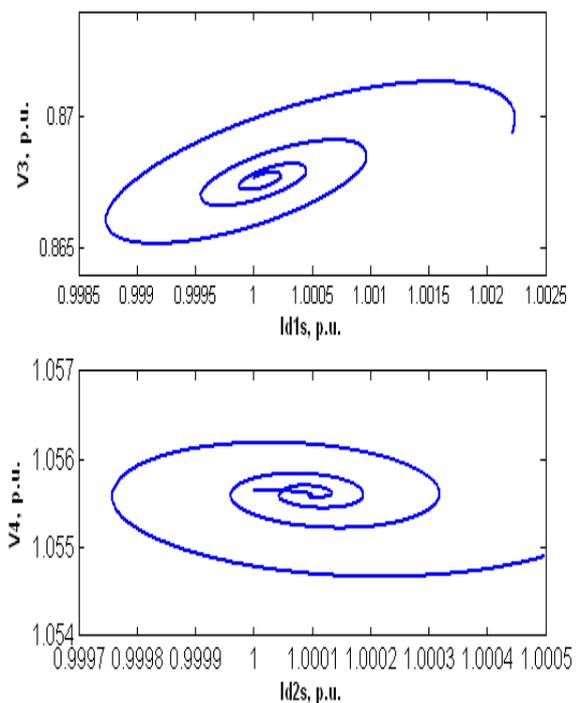Fig. 6-a. Time response of DC line current and voltage of the second DC line.

Fig. 6-b. Phase planes of (V_3, I_{d1s}) and (V_4, I_{d2s}).

Fig. 6. Unstable time responses and phase planes for 0.0001 step increase in 2nd line's current order (both lines on CDA/ CC, SCR_{Rects}=1.8702).
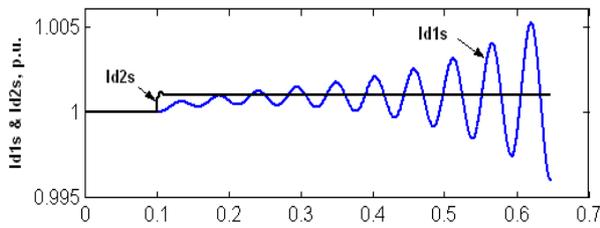
Fig. 7. Effect of adding 0.06 p.u. capacitor at rectifier of second DC line at SCR_{Rects} of 1.8702 (both DC lines operate on CDA/CC).
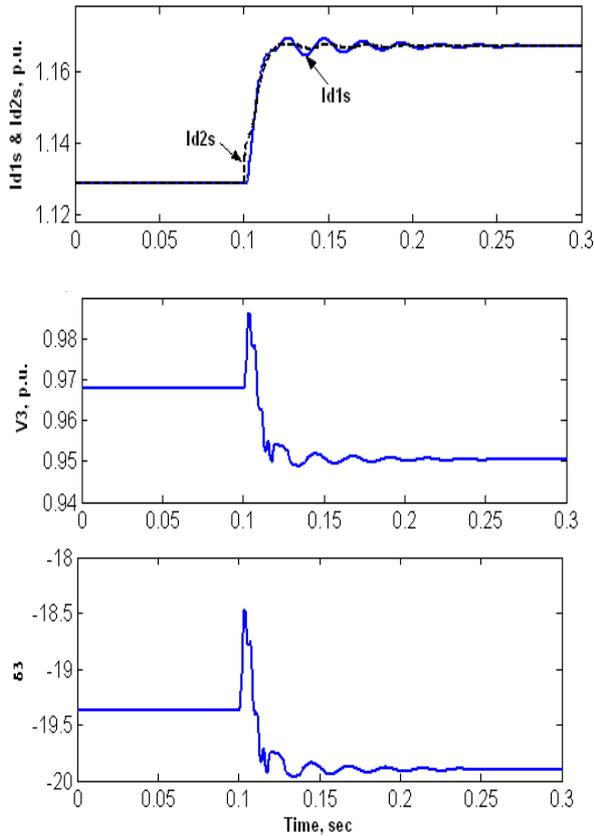

Fig. 8. Time responses of V_3 and δ_3 for control mode change from CDA/CP to CDA/CC with 0.001 step increase in 2nd DC line power order at SCR_{Rects} of 3.051572.

Fig. 9 illustrates the effect of SVC application at bus 3 on AC line voltages in terms of associated voltage stability factor. The shape of line voltages were improved and subsequently the DC line voltage stability factor. Without SVC, the system power flow failed to obtain solution at SCR_{Rects} of 3.051572 while with SVC the system remained stable at the same control mode up to SCR_{Rects} of 2.4230676. A significant improvement of

system voltage stability is thus attained by extending the adopted mode margin.

Fig. 10 compares between the system's performance without additional stability enhancement and its performance in either the presence of shunt DC line capacitance at rectifier and inverter line ends, operating an SVC or changing control mode of second DC line (after 20 msec) from CDA/CP to CDA/CC. The SCR_{Rects} =3.051572 and the power order of the second line encountered a 0.01 step increase at 0.1 sec. Stability is readily reached by either control mode transfer or applying an SVC. Nevertheless, adopted capacitor values failed to maintain system stability.
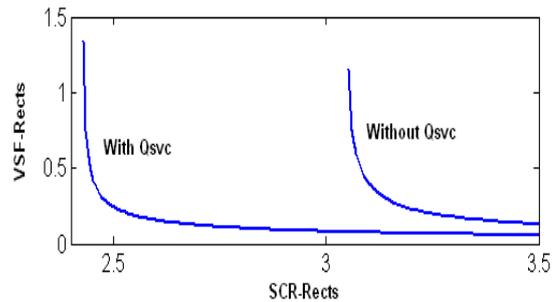

Fig. 9. Voltage stability factor at rectifier of 2nd line (1st line adopts CDA/CC and 2nd line adopts CDA/CP).
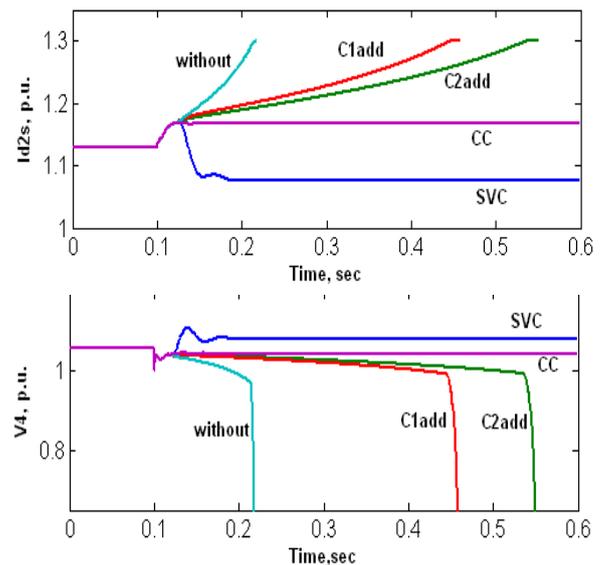

Fig. 10. Time responses with and without stability enhancement actions (1st line adopts CDA/CC and 2nd line initially adopts CDA/CP).

7. Conclusions

A novel detailed analysis of the performance of a multi-infeed HVDC system taking into account all possible combinations of control modes is proposed.

The interactions resulting from various changes in both lines were considered in the proposed model. The analysis defines the performance of the system from a voltage stability perspective making it possible to expect and issue timely corrective actions with suitable extent. Furthermore, the results show that operating several coordinated stability enhancement techniques allows for partially modifying the response and extending the control mode applicability by one technique in such a way to accept the adequate operation of other technique(s).

Appendix 1

MIF system data (p.u.)

R_{Lf}	L_{Lf}	C_{1f}	C_{2f}
0.0446	0.00082	0.00027	0.000272
$\bar{R}_{Ls}$	$\bar{L}_{Ls}$	$\bar{C}_{1s}$	C_{2s}
0.0446	0.00082	0.00027	0.000272
$\bar{Z}_{10}$	$\bar{Z}_{20}$	$\bar{Z}_{30}$	Z_{40}
0+j0.24	0+j0.333	0+j0.24	0+j0.333
$\bar{B}_{c1f}$	$\bar{B}_{c1s}$	$\bar{B}_{c2f}$	B_{c2s}
0.41	0.41	0.61	0.61

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