Design and implementation of parallel resonant electronic ballast with power factor correction

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High power factor electronic ballast is assessed in this work. The electronic ballast is able successfully to supply the fluorescent lamp assuring high power factor. Design of the active Power Factor Correction (PFC), is outlined. High power factor is obtained using a boost converter operating in Transition Mode (TM), resulting in high efficiency due to zero current switching. A self-excited half-bridge current fed parallel resonant inverter is designed and implemented. Experimental results of the system show high performance with the implemented ballast.

يتناول هذا البحث كيفية بناء خانق الكترونى للمبات الفلوروسنت و البحث يتكون من مرحلتين: المرحلة الأولى هى بناء متحكم فعال لتحسين معامل القدرة والمرحلة الثانيةهى بناء قلاب لتحويل التيار مستمر الى تيار متردد عالى الجهد والتردد وجيبى الشكل وله القدرة على اضاة عدد من اللمبات النيون ويعمل بنظرية الرنين الذاتى المتوازى. وتم التحقق من كفاءة التصميم عمليا من خلال عرض النتائج المعملية.

Keywords: Electronic ballast, Power factor correction, Resonant inverter, Fluorescent lamps

1. Introduction

Recently, the use of electronic ballast to supply fluorescent lamps is increasing rapidly due to the need of luminous efficacy, especially at high frequency. Nowadays an intensive work is being carried out to obtain low-cost and high efficiency topologies in order to implement electronic ballasts. Traditionally, the passive circuits, PFC, were chosen at nominal line frequency. Due to reasons of high weight and size, their use was limited. Moreover, the IEC1000-3-2 regulation [1] makes it necessary the use of Active Power Factor Correction (APFC), instead of other passive PFC. High Power Factor (HPF), and low Total Harmonic Distortion (THD), are specified features by international regulations and it is also recommended by utility companies to reduce the line current harmonics and rms value.

Typical implementation of two-stage electronic ballast is the boost converter followed by a half bridge inverter. Lately, several single-stage electronic ballasts with HPF have been proposed [2-3]. The task of this topology is to integrate HPF stage with high frequency inverter in one unit, thereby reducing the control circuit complexity. However the cost factor is the decision maker between single- and two-stage EBs. Fig. 1 shows two-stage electronic ballast for the fluorescent lamp, power factor correction unit followed by current-fed parallel resonant dc/ac inverter. The boost converter usually operates in Discontinuous Mode (DCM) for the low power rating and in Continuous Conduction Mode (CCM) for high power ballast.

2. The Electronic Ballast (EB)

The topologies for the EB inverter are either current fed or voltage fed versions. Cleaner sinusoidal waveforms are obtained with current fed inverter, hence high lamp efficacy is offered. Also the current fed scheme can drive a number of lamps in parallel, compared to single lamp capability with the voltage fed scheme.

The self-oscillating technique is employed in this work. As the electronic ballast based on self-oscillating technique possesses inherent current limiting control to the lamps usually operates at high resonant, frequency and yield high striking voltage. It can also

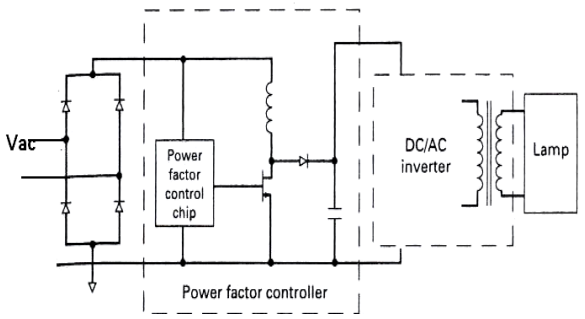

Fig. 1. Block diagram of a modern fluorescent lamp light source.

provide shutdown protection in case of lamp failure or removal [4]. The resonant inverters can serve as power stages of EB. Based on considerations of cost and component stress, typical inverter topologies such as half bridge series/parallel-loaded resonant inverter, push-pull inverters are broadly employed in EB design [5-[6].

HPF is achieved by using boost converter working in TM and operating in DCM, resulting in a lower dc-bus voltage than the one produced by conventional boost. In the following sections, theoretical analysis and experimental results are obtained for three fluorescent lamps, 25 Watt operating at 40 kHz switching frequency and 220 V.

3. Active Power Factor Correction unit, (APFC)

The main task of the APFC unit is to shape the input current in sinusoidal fashion and be in phase with the supply voltage. The power circuit of APFC could be divided into two major parts, the input diode bridge rectifier and the boost converter.

Firstly, the switching frequency should be chosen and accordingly the power chopper elements (inductor, power switch and the diode) are determined. Generally speaking, the boost converter is designed to operate above the audible range to allow the use of small components size and below few hundreds of kHz to keep high efficiency. The switching frequency is the reciprocal of the sum of the switching times given by [7]:

$$f_{sw} = 1 / [2P_o L(\frac{1}{V_{inrms}^2} + \frac{\sqrt{2}\sin(\omega t)}{V_{inrms}(V_o - V_{in\max}\sin(\omega t))})],$$

where P_o is the boost converter output power, L is the boost inductance, V_{in} is the input voltage and V_o is output DC voltage.

This frequency varies with line and load conditions. The maximum inductance for the boost inductor is set by the required minimum switching frequency and the minimum inductance is enforced by the minimum on time of the control IC. It was noted that designing the inductance value more on the maximum side helps improve the converter stability and reduce THD due to lower switching frequencies.

Based on the design equations obtained in [7], APFC circuit was designed and implemented. The application specs were 108-275 V input voltage, an output power of 130 W and maximum output voltage ripple of 20 V. The control IC was selected as STL6561 with transition mode operation. The bus voltage was selected as 400 V and the minimum switching frequency as 40 kHz. The resulting circuit is shown in fig. 2 with the components designations and values. Control components have been designed per the IC data sheet. Due to load variations, a compensation circuit was needed for the voltage error amplifier to ensure both low crossover frequency and adequate phase margin.

4. Electronic ballast circuit analysis

A self-excited half bridge parallel resonant electronic ballast (SEHBREB) designed for fluorescent lamp is illustrated in fig. 3. The circuit operation comprises two stages: start up and steady state. In the start up stage, components and lamps are subject to high voltage and /or current that would shorten the life time of lamp and deteriorate the reliability of inverters. However in the steady state, Current Crest Factor (CCF) of lamps,

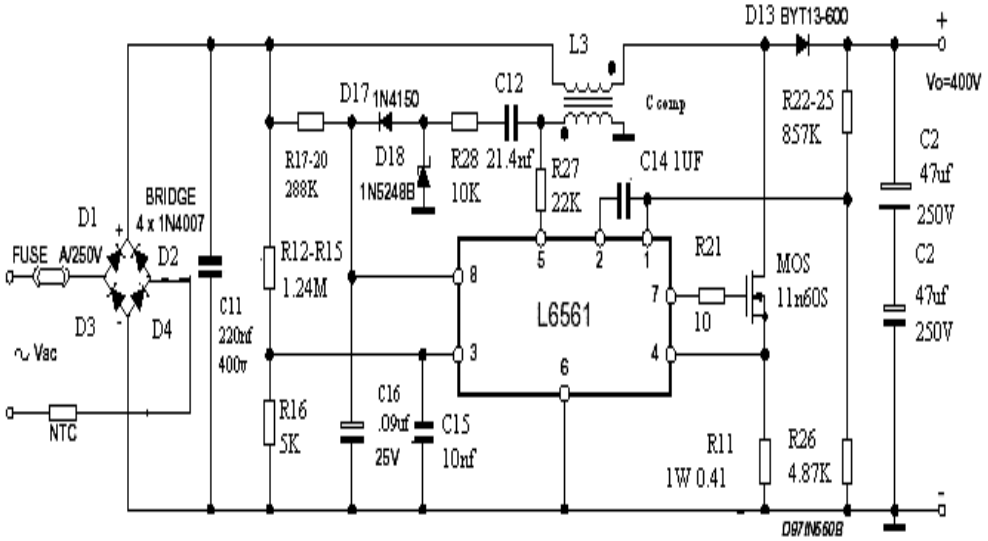

Fig. 2. The practical circuit of the 130 W power factor correction.

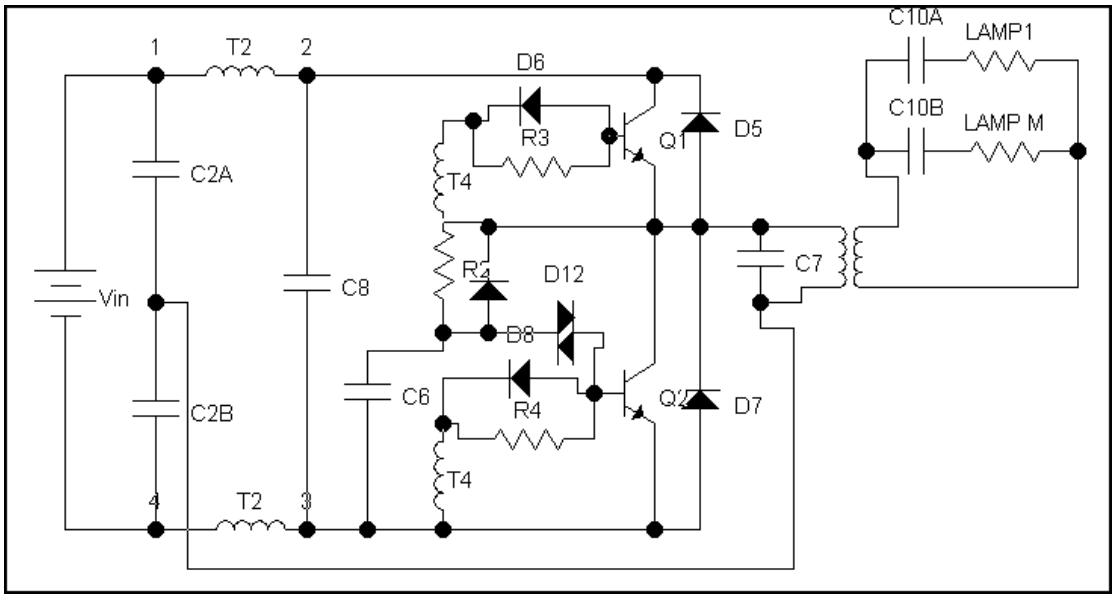

Fig. 3.Schematic diagram of a self-excited current-fed half-bridge parallel resonant electronic.

operating frequency and the time interval of dead zone are other factors which would affect the overall performance of the EBs. Therefore start-up and steady state should be considered in order to get an appropriate design of the EB and hence assuring optimized system performance. Generally speaking, each component plays multi-roles in these stages; thus several iterations and review based on a systematic design procedure are necessary to finish the tasks. The design procedures are based on the start-up and steady state analysis in [8].

5. Design example

Fig. 4 shows the complete circuit diagram for the electronic ballast.

Based on the previous description, the design procedure for the described electronic ballast can be as follows:

1. Determine the type of lamps and the number of lamps connected to the ballast.
The selected lamps are three of F40T12 type.
2. Measure the equivalent resistance (R_{lamps}) of the lamp, starting voltage, (V_{st}), operating voltage, (V_{op}) across the lamp and operating current I_{op}.
R_{lamps}=245, V_{st}=580 V V_{op}=104 VI_{op} = 0.43 mA
3. Select operational frequencies before and after lighting denoted by f_b and f_a, where $f_b > f_a$: f_b =130 kHz and f_a =120 kHz
V_s = 400 V the output from the power factor correction
4. Determine the turns ratio (N) of $T_{4\,(1\text{-}2)}$ to $T_{4\,(6-7)}$, fig. 4, from the following
Equation:

$$N = \frac{4V_{st}}{\pi V_s(1+2f\ T_d)}$$

T_d is about or less than 5% of the period T_a after operating the ballast

$$T_a = \frac{1}{F_a} = \frac{1}{120000} = 8.3\ \mu s$$

$T_d = 8.3 \times 0.02 = 0.17\ \mu s$ For ideal case T_d = 0

$$N = \frac{4 * 580}{\pi(400)(1+2\times 120000\times 0.17)} = 1.8$$

5. Determine C_{lamp} from the following equation:

$$C_{lamp} = \frac{V_{op}}{2\pi f_a R_{lamp}(V_{st} - V_{op})}$$

$$C_{lamp} = \frac{104}{2\pi 120000 \times 245 \times (580-104)} = 1.18334\ nF$$

Select C_{Lamp}= 1.2 nF

6. Choose C_{eff} (resonant capacitance) = 4C_8 + C_7 and L_{T4m} for satisfying the following:
7.

a) $$f_b = \frac{1}{2\pi\sqrt{C_{eff}\, L_{T4m}}}$$

C_{eff} = 4*, 62 + 4.7 = 7.18 nF

$$130000 = \frac{1}{2\pi\sqrt{7.18\times 10^{-9}\times L_{T4m}}}$$

L_{T4m} =0.21 mH

b) $$f_a = \frac{1}{2\pi\sqrt{(C_{eff} + MN^2\, C_{lamp})\, L_{T4m}}}$$

7. Determine the capacitor C_8 and C_7 when compromising the current and
Voltage stresses imposed on switching devices, lamp life, and radiated Electro-Magnetic Interference (EMI)
The values of, C_7 and C_8 are selected to satisfy the following inequality
2.5 C_8 < C_7 < 8 C8
2.5 (0.62) nf < 4.7nf < 8(0.62) nf
8. Design magnetizing inductance (L_{T2m}) of transformer T_2 (resonant Inductor) such that L_{T2m}>8 L_{T4m} L_{T2m}>8 ×0.21, Give L L_{T2m} = 2 mH
9. Design leakage inductances ($L_{T2Leakage}$ and $L_{T4Leakage}$) of transformer T_2 and T_4 so as the dead time is less than 5% of the period.
$T_d = 2\pi / \omega_{ds}$

$$0.17\times 10^{-6} = 2\pi/\omega_{ds}$$

$$\omega_{ds} = 2\pi/0.17\times 10^{-6} = 36941176\ \text{rad/s}$$

$$\omega_{ds} = \omega_{os}\sqrt{1-(\frac{1}{2Q_{ds}})^2}\quad \omega_{os} = \frac{1}{\sqrt{C_7 L_{T2leakage}}},$$

$$Q_{ds} = \frac{\sqrt{L_{T2\,leakage}/C_7}}{R_{T2}} > \frac{1}{2}$$

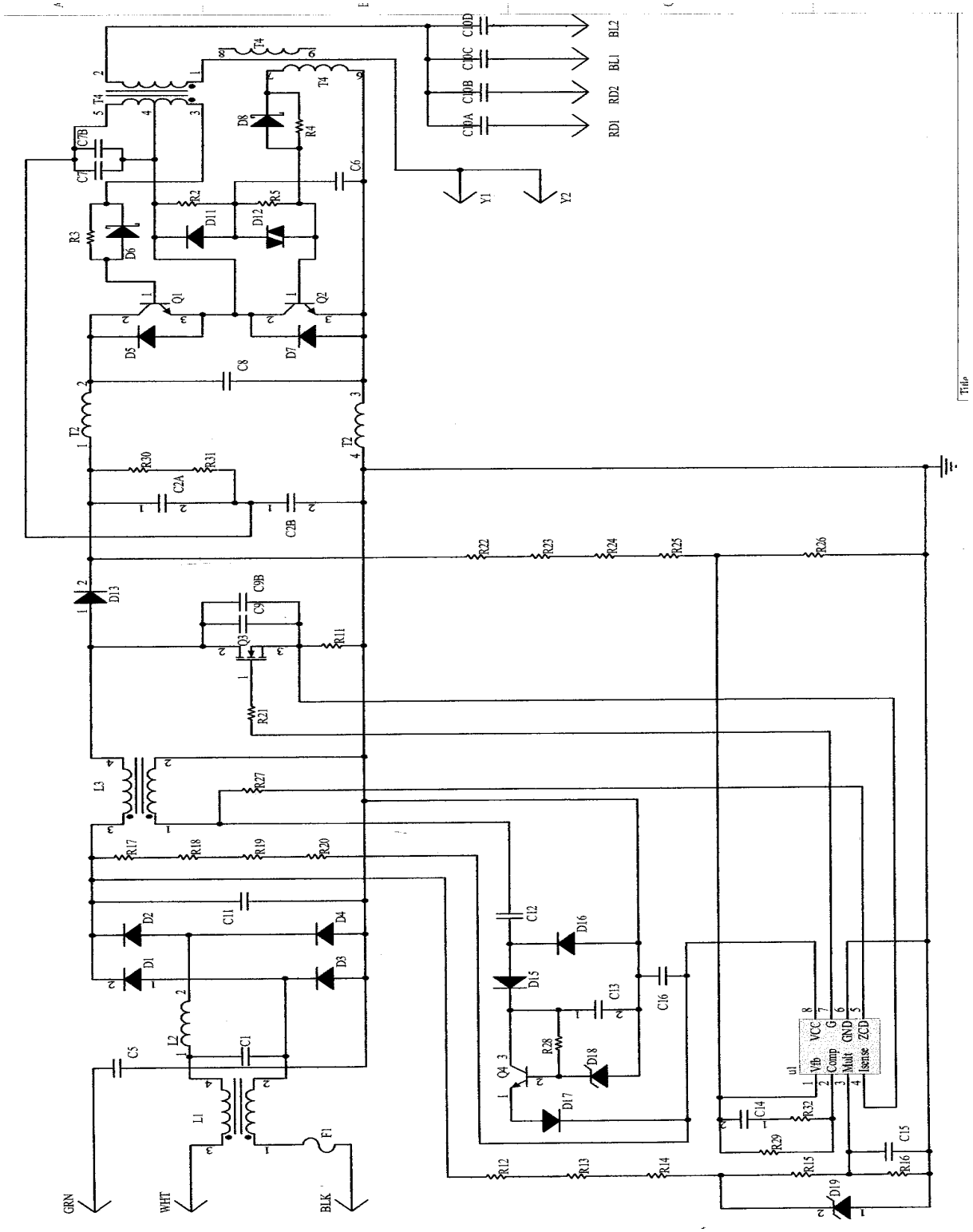

Fig. 4. The complete circuit diagram of the electronic ballast.

$$36941176 = \omega_{os}\sqrt{1-(\frac{1}{2\times 2})^2} \quad \text{for } Q = 2,$$

Then ω_{os} = 38152682 From

$$\omega_{os} = \frac{1}{\sqrt{4.7\times 10^{-9}\times L_{T2leakage}}} = 38152682 ,$$

Then L_{T2} leakage=0.14μH

Select also L_{T4} leakage= 0.14μH

From $Q_{ds} = \frac{\sqrt{L_{T2\,leakage}/C_7}}{R_{T2}} > \frac{1}{2}$, $\frac{\sqrt{0.14\times 10^{-6}/4.7\times 10^{-9}}}{R_{T2}} = 2$

then R_{T2} =2.78 OHM.

10. Determine the turns ratio K of $T_{4\ (6-7)}$ to $T_{4\ (4-5)}$ or $T_{4\ (3-4)}$ to $T_{4\ (4-5)}$, fig. 4, and current limiting resistor to insure that Q_1 and Q_2 can be driven into saturation mode and have a proper dead time.
11. Select transistors type $Q1$ and $Q2$ ($T1103$ EBT) or (2SD1402).
12. It might need several iterations from step 3 to 10.

5. Results

After having design the EB using the design equations in the previous sections, a prototype has been tested. The results of the system with the ballast are shown in this section; fig. 5 shows the lamp voltage. The starting voltage is reaching 500 volts, and then it goes down to the operating voltage. In the same manner the dc link current behaves as shown in fig. 6. While the transistor current, fig. 7 is very small in the beginning and it goes up after the lamp operation. The inverter output voltage behaves in a sinusoidal fashion after the lamp breakdown, fig. 8. Also the inverter voltage at no load is around 500 volts, shown in fig. 9. High power factor (almost unity) is assured in fig. 10, as the supply current has a sinusoidal waveform and in phase with the supply voltage, fig. 11. Finally, fig. 12 gives the gate control signal of the MOSFET. The output voltage of the 130-watt APFC, fig. 13, is almost constant with a very small percentage ripple.

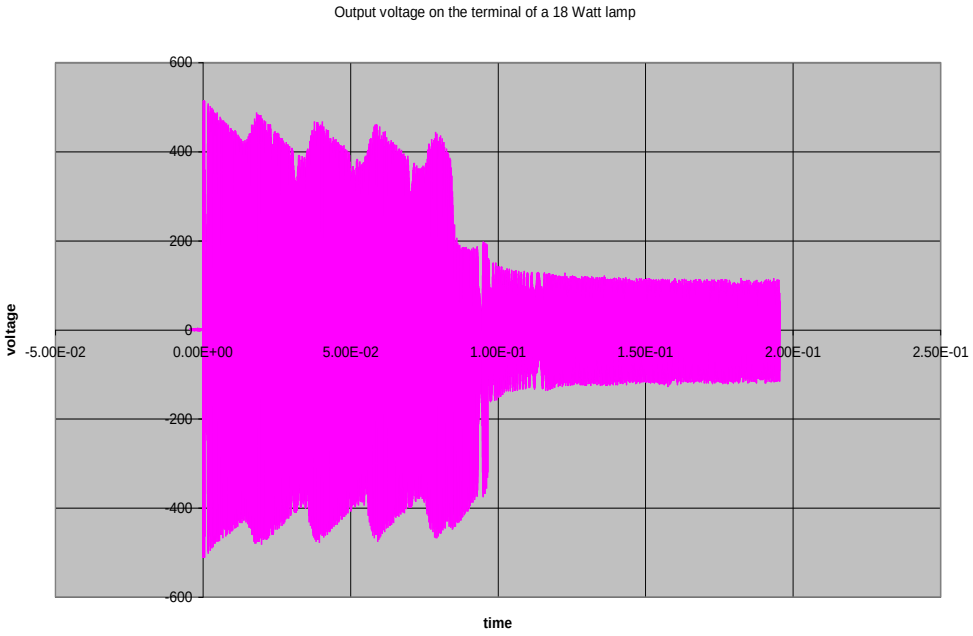

Fig. 5. the electronic ballast output voltage, before and after break down.

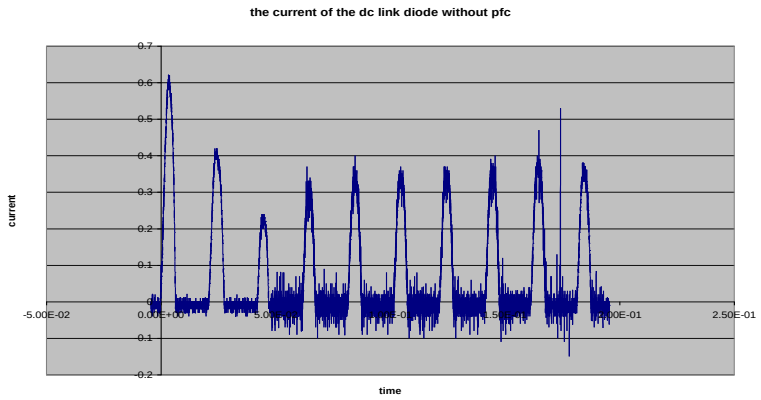

Fig .6 The current waveform of the DC link diode D_{13} with PFC.

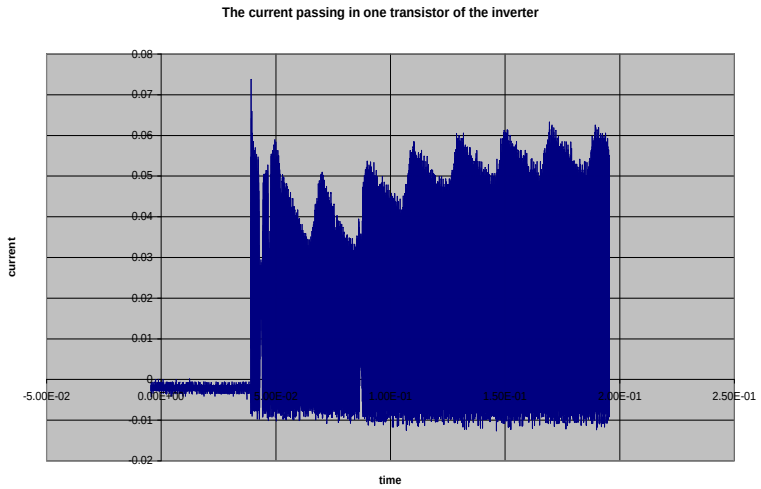

Fig. 7. The transistor current before and after the lamp operation.

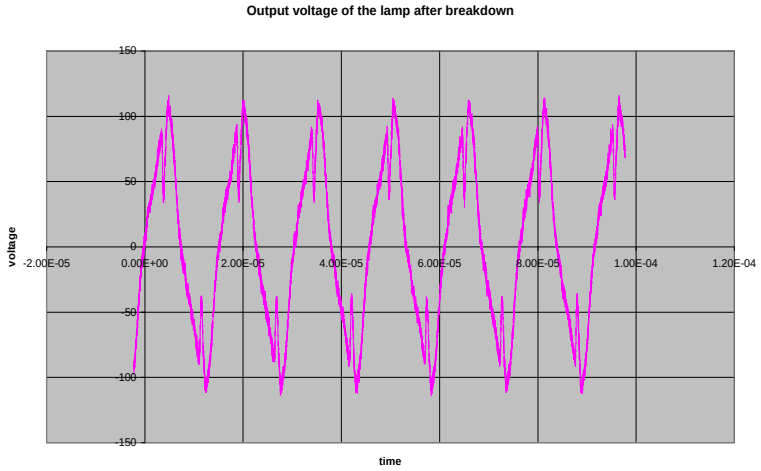

Fig. 8. The transistor current before and after.

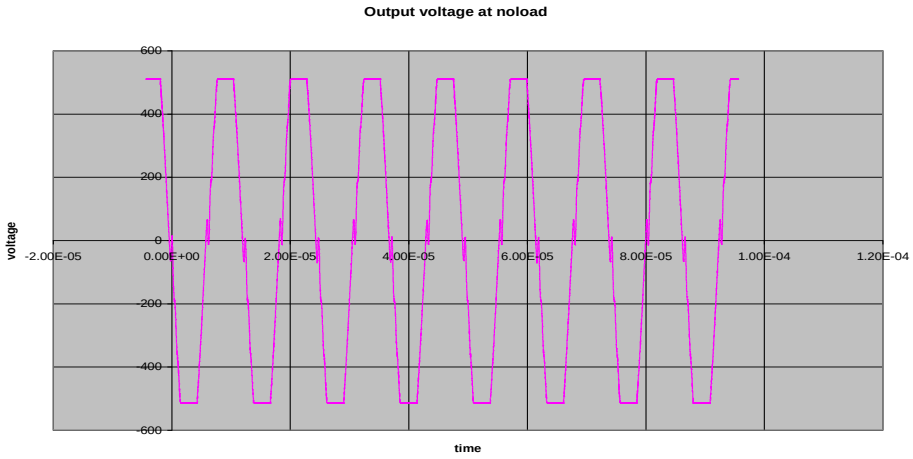

Fig. 9 Output voltage of the inverter at no load.

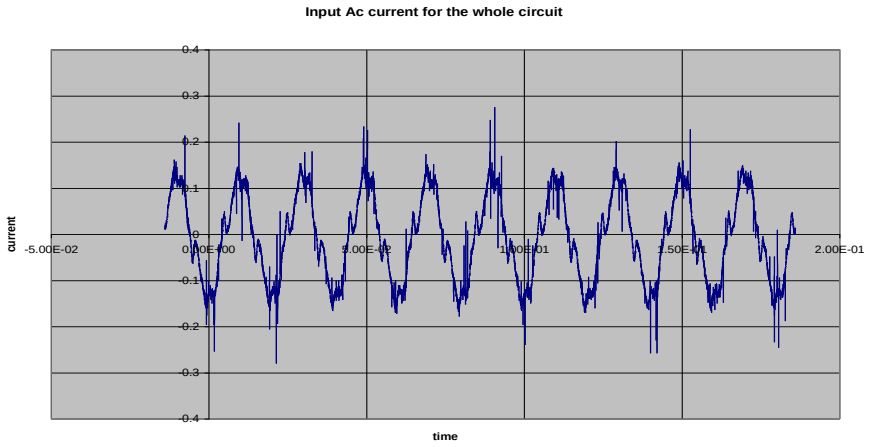

Fig. 10. The ac input line current.

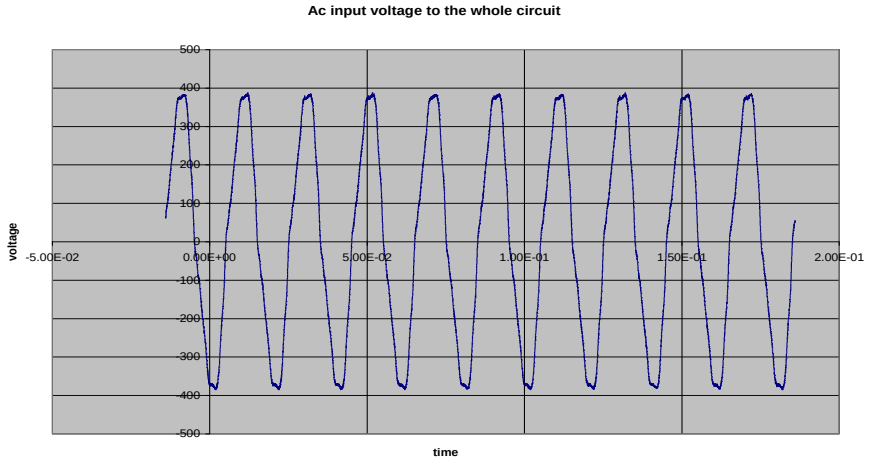

Fig.11. the input ac line voltage.

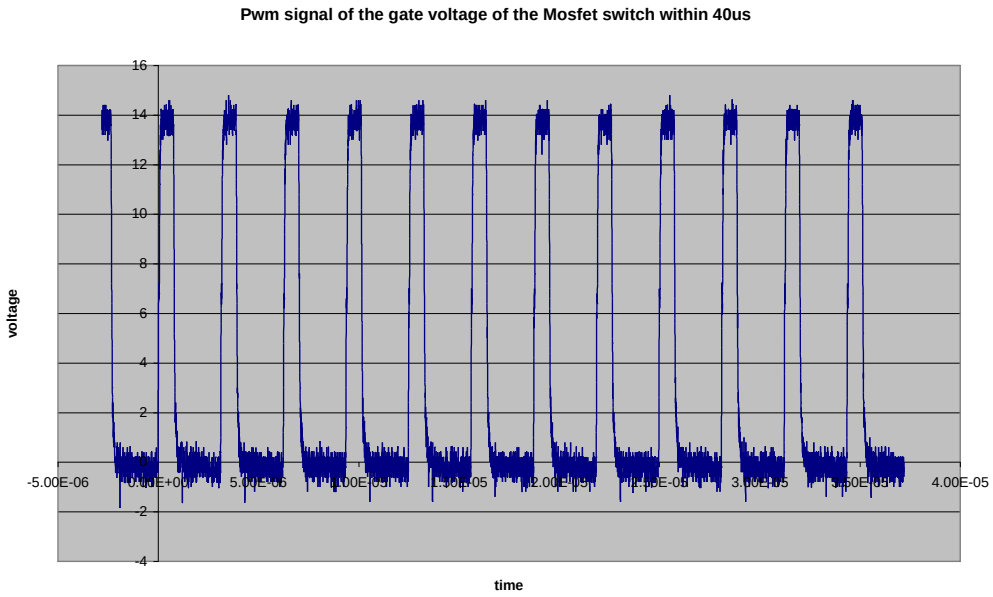

Fig. 12 the gate control signal (PWM) of a MOSFET within 40μS.

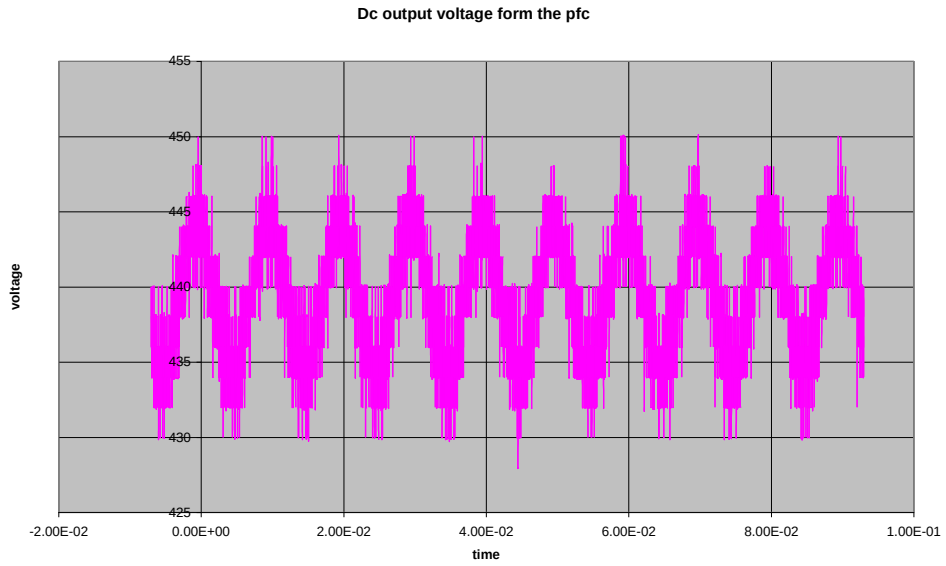

Fig. 13. Output DC voltage of the power factor correction unit.

6. Conclusions

This work has dealt with the design implementation of SEHPPR electronic ballast. The EB is a two-stage version, APFC followed by a half-bridge parallel resonant inverter. The APFC was used to provide unity power factor and low THD. The resonant inverter ignited and supplied the lamps at the nominal operating points. The design procedures of both APFC and resonant inverter based theoretical equations and practical considerations were assessed. Finally a proto-type of EB was implemented and experimental results

show excellent performance with the electronic ballast. The ballast is able to supply the lamp assuring unity power factor and low THD for the utility line.

References

[1] "IEC 1000-3-2 (1995-03) Standards on Electromagnetic Compatibility (EMC), Part 3, Section 2: Limits for Harmonic Current Emissions", International Electro-Technical Commission, Geneva, Switzerland, Apr. (1995).

[2] A.J. Calleja, J.M. Alonso, E. loez and ..., "Analysis and Experimental Results of a Single-Stage High Power Factor Electronic Ballast Based on Flyback Converter", IEEE Trans. Power Electronics, Vol. 14 (6), pp 998-1006 (1999).

[3] J. Qian, F.C. Lee and T. Yamauchi," An Improved Charge Pump Power Factor Correction Electronic Ballast", IEEE Trans. Power Electronics, Vol. 14 (6), pp. 1007-1013 (1999).

[4] Márcio Almeida Có, Domingos, S.L. Simonetti, and Jose Luiz. "High-Power-Factor Electronic Ballast Based on a Single Power Processing Stage"., IEEE Trans. Industrial electronics, Vol. 47 (4) (2000).

[5] M.C. Cosby and R.M. Nelms, "Designing a Parallel-Loaded Resonant inverter for an Electronic Ballast Using the Fundamental Approximation, " Proceedings of APEC" 93, San Die go, CA. pp.418-423.

[6] T.-H. Yu, L.-M. Wu and T.-F. Wu, "Comparisons among Self-Excited Parallel Resonant, Series Resonant and Current-Fed Push-Pull Electronic Ballasts", Proceedings of APEC, 94 Orlando, FL, pp. 421-426 (1994).

[7] Amr. A. Ghazala, "Active Power Factor Correction for Medium Power Switching Mode Power Supply", MEPCON, Egypt (2001).

[8] T.-F. Wu, T. - H. Yu, and H. -M.Huang "Complete Analysis and Performance-Characteristic Compromise for Self-Excited Half-Bridge Parallel Resonant Electronic Ballast", Proceeding of PESC, pp.124- (1994).

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