Performance evaluation of blocking ATM switches
(I) uniform traffic case

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Discrete time queueing systems had been extensively used in the analysis of buffer behavior in computer communication systems. Currently, discrete time queueing systems are used in the analysis of computer and communication networks working under the Asynchronous Transfer Mode (ATM) technology. A distinct feature of this technology is that the basic cell (called ATM cell) containing data and routing information has a fixed size. Thus, the time required to transmit such cells within the same system is constant and can be considered as the basic time slot. In this paper, we consider a blocking ATM switch where both internal blocking and output port blocking are encountered by incoming cells. The switch is investigated under a general arrival stream and uniform output port distributions. It is assumed that the switch is provided with internal output buffers. Analytical expressions for utilization, occupation and delay of every internal buffer as well as total delay through the switch are computed to add new general results to the existing special ones in the literature. Moreover, simulation is used to compute cell loss probability for switches with finite buffers. An important result, from a practical point of view, is obtained, namely that, a small loss probability can be achieved with a small buffer size.

استخدمت أنظمة الطوابير ذات الزمن المتقطع في تحليل أداء حواجز الانتظار الموجودة في أنظمة اتصالات الحاسبات. والآن تستخدم هذه الأنظمة في تحليل شبكات الحاسب وشبكات الاتصالات التي تعمل بتقنية نظام التحويل الغير متزامن (ATM). وهذه التقنية تتميز بأن الخلية الأساسية التي تحوي البيانات ومعلومات المرور خلال الشبكة لها طول ثابت. ومن ثم يكون الزمن اللازم لنقل هذه الخلايا زمنا ثابتا يعتبر هو وحدة الزمن الأساسية. في هذه المقالة ندرس أحد المفاتيح الموجودة في الشبكات العاملة بهذه التقنية. وهذا المفتاح به اعتراضات داخلية وكذلك اعتراضات عند المخارج. نفترض أن عملية الوصول العشوائية عملية عامة والمرور خلال المفتاح منتظم. وكذلك نفترض أن المفتاح به حيز انتظار لانهائي عند المخارج الداخلية. وقد تم الحصول على صيغ مضبوطة لمعامل الاستغلال ومعدل الإشغال وزمن الانتظار لكل حيز انتظار وكذلك صيغة مضبوطة لزمن الانتظار الكلى للمفتاح. بالإضافة إلى ذلك تم استخدام المحاكاة لحساب احتمال فقد الخلايا في حالة للمفاتيح التي تعمل بحيز انتظار ذو سعة محدودة.

Keywords: Discrete time queueing systems, Blocking ATM switches, Internal output buffers

1. Introduction

Discrete time queueing systems had been extensively used in the analysis of buffer behavior in computer communication systems [1-4]. Currently, discrete time queueing systems are used in the analysis of computer and communication networks working under the Asynchronous Transfer Mode (ATM) technology [5-7]. A distinct feature of this technology (as opposed to other packet switching techniques) is that the basic cell (called ATM cell) containing data and routing information has a fixed size. Thus, the time required to transmit such cells within the same system is constant and can be considered as the basic time slot. ATM switches are divided into two basic categories: blocking switches and non-blocking switches. In a non-blocking switch, no internal blocking is encountered by arriving cells. However, cells may suffer from output port contention. In a blocking switch, both internal blocking and output port blocking are encountered by incoming cells. Nevertheless, a blocking switch has a superior reduction in the number of switching elements required to implement it.

In this paper, we use a discrete time queueing system model to analyze a blocking ATM switch based on a banyan network structure [8,9]. Banyan networks are usually provided with one or more performance enhancement techniques [8-11]. In [12], a Banyan network with infinite output queueing

was analyzed where it was shown that a maximum throughput of one can be achieved. However, infinite buffer size assumption is not suitable for practical implementation. Hence, in [13], the finite output buffer case was considered. With special implementation to take care of the overflow problem, it was shown [13] that a maximum throughput of one can again be achieved. In the present work, we assume infinite buffer size for the analytic analysis. Moreover, a simulation study is presented for switches with finite buffer sizes. The analysis of ATM switches is affected by the assumption on the arrival stream. Bernoulli arrivals is a common assumption [12,13]. In the present work, we assume general arrival stream which includes the Bernoulli arrivals as a special case. Another important feature of the switch model is the traffic pattern which describes the chance of an incoming cell to be assigned to different output ports. In uniform traffic, output ports have equal chance. This assumption was employed in [12,13] and will be used in the present work. The non-uniform traffic case where output ports have different chances is readily analyzed and will appear in another paper.

Exact expressions for the utilization, occupation and delay of every internal queue as well as an analytical expression for the total delay through the switch are derived. Infinite buffer assumption is assessed by computing the maximum expected queue length. It is noticed that the expected queue length doesn't exceed a small finite value for almost all the working loads. Cell loss probability (for switches with finite buffers) is estimated using simulation. It is verified that a small loss probability can be achieved with a small buffer size

The rest of this paper is organized as follows: In Section 2, we state the model description and introduce the notations that will be used throughout this work. The analytical analysis appears in Section 3 and numerical results are presented in Section 4. Conclusion and some open problems are given in Section 5.

2. Model description

Consider an $N{\times}N$ ATM switch which is built using a baseline Banyan network **Error! Reference source not found.**[*14*] consisting of log_2N stages where each stage has $N/2$ binary switching elements. An example for $N = 8$ is shown in fig. 1. Assume that the arrival stream to input port i, $1 \le i \le N$, is represented by the time stationary stochastic process $\{A_i(n), n \ge 1\}$ with moments $\overline{A_i} = E(A_i(n))$ and $\overline{A_i^2} = E(A_i^2(n))$. Assume that a cell arriving at input port i is destined for output port j with probability r_{ij}, $1 \le i, j \le N$. Throughout this work, we assume uniform output distribution, i.e., $r_{ij} = 1/N$, $1 \le i, j \le N$. A parallel study concerning non-uniform traffics is readily analyzed and will appear in another paper. The arrival streams and the routing probabilities are assumed to be mutually independent. The Banyan network is provided with internal output buffers with infinite capacity as shown in fig. 2. The switching element fabric runs twice as fast as the input and output ports of the switch in order to be able to deliver two incoming cells (with the same output link destination) to the required output queue during one time slot.

Define $A_{i,j}(n)$ as the number of ATM cells that arrive during the nth time slot to input link j located at stage i of the Banyan network where $1 \le i \le log_2 N$, $1 \le j \le N$. Similarly, define $B_{i,j}(n)$ as the number of ATM cells that arrive during the nth time slot to the queue located at output link j and stage i. Denote that queue by $b_{i,j}$. Finally, define $C_{i,j}(n)$ as the number of ATM cells departing from the buffer $b_{i,j}$ during the nth time slot. The late arrival scheme is assumed [15]. The processes $A_{i,j}(n)$, $B_{i,j}(n)$ and $C_{i,j}(n)$ are illustrated in fig. 2. Let the first and second steady state moments of these processes be denoted by $\overline{A_{i,j}}, \overline{A_{i,j}^2}, \overline{B_{i,j}}$ $\overline{B_{i,j}^2}, \overline{C_{i,j}}$ and $\overline{C_{i,j}^2}$, respectively.

3. Analytical analyss

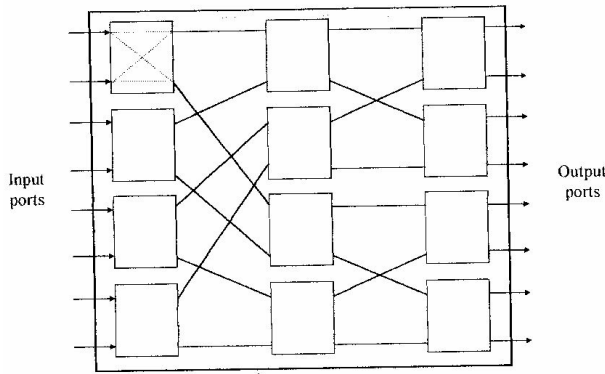The uniform output distribution implies a uniform distribution at each stage of the

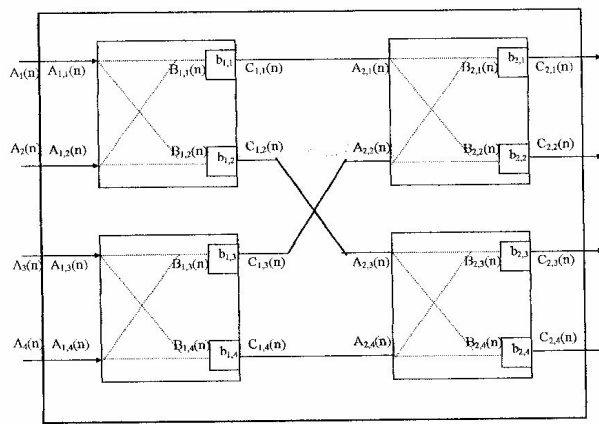Fig. 1. An 8 ×8 Banyan network based ATM switch.

Fig. 2. Internal output queuing in a 4×4 Banyan network based ATM switch.

banyan network. More specifically, the incoming cell to a switching element chooses between the two output links with equal probabilities. Dfine the indicator function $I_{k,j}^{i}(n)$, $1 \le i \le log_2 N$, $1 \le k, j \le N$, as follows:

$I_{k,j}^{i}(n) = 1$,   if cells that arrive during the nth time slot at the input link k of stage i are directed to the output link j

= 0,   otherwise

The process $I_{k,j}^{i}(n)$ is a Bernoulli process with a success probability 0.5 whenever k and j belong to the same switching element.

Analytical expressions for the moments $\overline{B_{i,j}}, \overline{B_{i,j}^{2}}$, $1 \le j \le N$, at the first stage of the

Banyan network are given in the following lemma:

Lemma 1

In the described blocking ATM switch the steady state first and second moments of the processes $B_{1,j}(n)$, $1 \le j \le N$, are given by:

$$\overline{B_{1,j}} = \frac{1}{2} \sum_{k \in \theta(j)} \overline{A_k}, \tag{1}$$

$$\overline{B_{1,j}^{2}} = \frac{1}{2} \sum_{k \in \theta(j)} \overline{A_k^{2}} + \frac{1}{4} \sum_{k1 \in \theta(j)} \sum_{\substack{k2 \in \theta(j) \\ k2 \neq k1}} \overline{A_{k1}} \, \overline{A_{k2}} \tag{2}$$

where $\theta(j) = \{k \mid A_{i,k}(n)$ is an input process to the switching element containing buffer $b_{i,j}\}$.

Proof:

Consider the first stage of the banyan network at which $A_{1,j}(n) = A_j(n)$, $1 \le j \le N$. Hence,

$$B_{1,j}(n) = \sum_{k \in \theta(j)} A_{1,k}(n) I_{k,j}^{1}(n) = \sum_{k \in \theta(j)} A_k(n) I_{k,j}^{1}(n)$$

Taking the expectation of both sides and noting that $A_k(n)$ and $I_{k,j}^{1}(n)$ are independent, then:

$$E(B_{1,j}(n)) = \sum_{k \in \theta(j)} E(A_k(n)) E(I_{k,j}^{1}(n)).$$

Noting that $A_k(n)$ and $I_{k,j}^{1}(n)$ are both time stationary and $E(I_{k,j}^{1}(n)) = 0.5$, then eq. (1) follows. Similarly,

$$B_{1,j}^{2}(n) = \left(\sum_{k \in \theta(j)} A_k(n) I_{k,j}^{1}(n) \right)^2$$

$$= \sum_{k \in \theta(j)} A_k^{2}(n) I_{k,j}^{1}(n) +$$

$$\sum_{k1 \in \theta(j)} \sum_{\substack{k2 \in \theta(j) \\ k2 \neq k1}} A_{k1}(n) A_{k2}(n) I_{k1,j}^{1}(n) I_{k2,j}^{1}(n)$$

Taking the expectation of both sides, gives eq. (2).

Remark:

The set $\theta(j)$ can be defined as follows:

$\theta(j) = \alpha(\lfloor (j-1)/2 \rfloor + 1)$, where $\alpha(q) = \{2q-1, 2q\}$ and $\lfloor q \rfloor$ denotes the floor of q.

Moreover, the set $\theta(j)$ can be generated algorithmically as follows:

Algorithm 1
function $\theta(j)$
    if j is odd then return $(j, j+1)$
    else return $(j-1, j)$
end.

Obtaining the performance measures of queues $b_{i,j}$ depends on the following theorem [16]:

Theorem 1: (Performance measures of the batch arrivals-geometric service queue)

For a discrete time queue having:

1. Arrivals that are represented by a time stationary stochastic process $\{A(n), n \geq 1\}$.
2. A single server with a geometric service time of parameter σ.

Then, the steady state utilization, occupation and delay are given, respectively, by:

$$E(W) = \frac{\overline{A}}{\sigma}, \qquad (3)$$

$$E(X) = \frac{\overline{A} + \overline{A^2} - 2(\overline{A})^2}{2(\sigma - \overline{A})}, \qquad (4)$$

$$E(D) = \frac{1}{\overline{A}} E(X) = \frac{\overline{A} + \overline{A^2} - 2(\overline{A})^2}{2\overline{A}(\sigma - \overline{A})}, \qquad (5)$$

where $\overline{A} = E(A(n))$ and $\overline{A^2} = E(A^2(n))$.

The performance measures of the queues $b_{1,j}$, $1 \leq j \leq N$, can now be computed using the above theorem as follows.

Theorem 2:
(Performance measures for the first stage)

The steady state utilization, occupation and delay of the jth output queue, $1 \leq j \leq N$, at the first stage of the described blocking ATM switch are given, respectively, by:

$$E(W_{1,j}) = \overline{B_{1,j}} \qquad (6)$$

$$E(X_{1,j}) = \frac{\overline{B_{1,j}} + \overline{B_{1,j}^2} - 2(\overline{B_{1,j}})^2}{2(1 - \overline{B_{1,j}})}, \qquad (7)$$

$$E(D_{1,j}) = \frac{\overline{B_{1,j}} + \overline{B_{1,j}^2} - 2(\overline{B_{1,j}})^2}{2\overline{B_{1,j}}(1 - \overline{B_{1,j}})}, \qquad (8)$$

where $\overline{B_{1,j}}, \overline{B_{1,j}^2}$ are given by eqs. (1) and (2).

Proof:

Each queue $b_{1,j}$ is a batch arrivals-geometric service queue whose arrival process is $B_{1,j}(n)$ and whose service probability equals one. Thus, the utilization, occupation and delay expressions follow from eqs. (3), (4) and (5), respectively.

In order to analyze the other stages, we have to identify the departure processes $C_{i,j}(n)$, $1 \leq i \leq (log_2 N) - 1$, $1 \leq j \leq N$. Moreover, we have to assign every $C_{i,j}(n)$ to the appropriate $A_{i+1,k}(n)$ according to the routing implied by the structure of the baseline banyan network. Tackling these two tasks will now be described.

Since each buffer $b_{i,j}$ is a single server queue, then the departure processes $C_{i,j}(n)$ are Bernoulli processes. Moreover, since the service probability at each buffer equals one and late arrival scheme is assumed, then the steady state departure rate equals $E(W_{i,j})$. Thus,

$$\overline{C_{i,j}} = \overline{C_{i,j}^2} = E(W_{i,j}), 1 \leq i \leq log_2 N, 1 \leq j \leq N. \qquad (9)$$

In order to assign each $C_{i,j}(n)$ to the appropriate $A_{i+1,k}(n)$, we define the map $\psi(i,j)$, $1 \leq i \leq (log_2 N) - 1$, $1 \leq j \leq N$ such that $A_{i+1,j}(n) = C_{i,\psi(i,j)}(n)$. In other words, $\psi(i,j)$ is the output link number at stage i to which the input link j at stage $i+1$ is connected. The following algorithm is used to generate $\psi(i,j)$:

Algorithm 2
function $\psi(i,j)$
begin
$\ell = (log_2 N) - i$ // ℓ counts in the reverse order
$s = 2^{\ell+1}$ // Module size

a = (j – 1) div s // Number of increments when modules are connected
j = ((j – 1) mod s) + 1   // Convert to the basic module
if ($j \leq s/2$) then $k = 2j – 1$ // Odd k's are sent to the next upper half
else $k = 2(j – s/2)$ // Even k's are sent to the next lower half
$k = k + a \times s$ // Add the required increments
return (k)
end.
For example, when N = 16 then the matrix [$\psi(i,j)$] equals:

$$\begin{bmatrix} 1 & 3 & 5 & 7 & 9 & 11 & 13 & 15 & 2 & 4 & 6 & 8 & 10 & 12 & 14 & 16 \\ 1 & 3 & 5 & 7 & 2 & 4 & 6 & 8 & 9 & 11 & 13 & 15 & 10 & 12 & 14 & 16 \\ 1 & 3 & 2 & 4 & 5 & 7 & 6 & 8 & 9 & 11 & 10 & 12 & 13 & 15 & 14 & 16 \end{bmatrix}$$

Identifying the departure processes $C_{i,j}(n)$ and establishing the map $\psi(i,j)$, we can analyze the buffers $b_{i,j}$ at other stages, $2 \leq i \leq log_2\ N$. To obtain the required performance measures at these stages, we start by computing the moments of the processes $B_{i,j}(n)$, $2 \leq i \leq log_2\ N$, $1 \leq j \leq N$.

Lemma 2:

In the described blocking ATM switch the steady state first and second moments of the processes $B_{i,j}(n)$, $2 \leq i \leq log_2 N$, $1 \leq j \leq N$, are given by:

$$\overline{B_{i,j}} = \frac{1}{2} \sum_{k \in \theta(j)} E(W_{i-1,\psi(i-1,k)}), \tag{10}$$

$$\overline{B_{i,j}^2} = \frac{1}{2} \sum_{k \in \theta(j)} E(W_{i-1,\psi(i-1,k)}) + \frac{1}{4} \sum_{\substack{k1 \in \theta(j) \\ }} \sum_{\substack{k2 \in \theta(j) \\ k1 \neq k2}}$$
$$E(W_{i-1,\psi(i-1,k1)}) E(W_{i-1,\psi(i-1,k2)}), \tag{11}$$

Proof:

From the definitions of $C_{i,j}(n)$ and $\psi(i,j)$, we can write the following relation:

$$B_{i,j}(n) = \sum_{k \in \theta(j)} A_{i,k}(n) I_{k,j}^i(n)$$
$$= \sum_{k \in \theta(j)} C_{i-1,\psi(i-1,k)}(n) I_{k,j}^i(n)$$

Taking expectation of both sides, considering the steady state and applying eq. (9), give eq. (10).

Similarly,

$$B_{i,j}^2(n) = \left(\sum_{k \in \theta(j)} A_{i,k}(n) I_{k,j}^i(n) \right)^2$$
$$= \left(\sum_{k \in \theta(j)} C_{i-1,\psi(i-1,k)}(n) I_{k,j}^i(n) \right)^2$$
$$= \sum_{k \in \theta(j)} C_{i-1,\psi(i-1,k)}^2(n) I_{k,j}^i(n)$$
$$+ \sum_{k1 \in \theta(j)} \sum_{\substack{k2 \in \theta(j) \\ k1 \neq k2}} C_{i-1,\psi(i-1,k1)}(n) C_{i-1,\psi(i-1,k2)}(n)$$
$$I_{k1,j}^i(n) I_{k2,j}^i(n)$$

Taking expectation of both sides, considering the steady state and applying eq. (9), give eq. (11).

Using the expressions given by eqs. (10) and (11), the performance measures of the queues $b_{i,j}$, $2 \leq i \leq log_2\ N$, $1 \leq j \leq N$, can be computed using *Theorem 1*.

Theorem 3: (Performance measures for the ith stage, $2 \leq i \leq log_2\ N$)

The steady state utilization, occupation and delay of the *j*th output queue, $1 \leq j \leq N$, at the *ith* stage, $2 \leq i \leq log_2\ N$, of the described blocking ATM switch are given, respectively, by:

$$E(W_{i,j}) = \overline{B_{i,j}}, \tag{12}$$

$$E(X_{i,j}) = \frac{\overline{B_{i,j}} + \overline{B_{i,j}^2} - 2(\overline{B_{i,j}})^2}{2(1 - \overline{B_{i,j}})}, \tag{13}$$

$$E(D_{i,j}) = \frac{\overline{B_{i,j}} + \overline{B_{i,j}^2} - 2(\overline{B_{i,j}})^2}{2\overline{B_{i,j}}(1 - \overline{B_{i,j}})}, \tag{14}$$

where $\overline{B_{i,j}}, \overline{B_{i,j}^2}$ are given by eqs. (10) and (11).

Proof:

See the proof of *Theorem 2*.

In fact, using eq. (12) we can simplify eqs. (10) and (11) to the following recursive form:

Corollary 1:

In the described blocking ATM switch the steady state first and second moments of the processes $B_{i,j}(n)$, $2 \leq i \leq log_2 N$, $1 \leq j \leq N$, are given by:

$$\overline{B_{i,j}} = \frac{1}{2} \sum_{k \in \theta(j)} \overline{B_{i-1,\psi(i-1,k)}}, \tag{15}$$

$$\overline{B_{i,j}^2} = \frac{1}{2} \sum_{k \in \theta(j)} \overline{B_{i-1,\psi(i-1,k)}} + \frac{1}{4} \sum_{k1 \in \theta(j)} \sum_{\substack{k2 \in \theta(j) \\ k1 \neq k2}} \overline{B_{i-1,\psi(i-1,k1)}} \; \overline{B_{i-1,\psi(i-1,k2)}}, \tag{16}$$

where $\overline{B_{1,j}}$ is given by eq. (1).

Example 1

If $A_1(n)$, $A_2(n)$,..., $A_N(n)$ follow a common stochastic process $A(n)$ with moments $\overline{A} = E(A(n))$, $\overline{A^2} = E(A^2(n))$, then eqs. (1) and (2) reduce to:

$$\overline{B_{1,j}} = \overline{A}, \tag{17}$$

$$\overline{B_{1,j}^2} = \overline{A^2} + \frac{1}{2}(\overline{A})^2, \tag{18}$$

where $1 \leq j \leq N$.

Establishing the above simple form of $\overline{B_{1,j}}$, the recursion formulas given in eqs. (15) and (16) can be solved to give:

$$\overline{B_{i,j}} = \overline{A}, \tag{19}$$

$$\overline{B_{i,j}^2} = \overline{A} + \frac{1}{2}(\overline{A})^2, \tag{20}$$

where $2 \leq i \leq log_2 N$, $1 \leq j \leq N$.

Using eqs. (17), (18), (19) and (20), the performance measures of the buffers $b_{i,j}$, $1 \leq i \leq log_2 N$, $1 \leq j \leq N$, are given by:

$$E(W_{1,j}) = \overline{A}, \tag{21}$$

$$E(X_{1,j}) = \frac{2\overline{A} + 2\overline{A^2} - 3(\overline{A})^2}{4(1 - \overline{A})}, \tag{22}$$

$$E(D_{1,j}) = \frac{2\overline{A} + 2\overline{A^2} - 3(\overline{A})^2}{4\overline{A}(1 - \overline{A})}, \tag{23}$$

$$E(W_{i,j}) = \overline{A} \tag{24}$$

$$E(X_{i,j}) = \frac{4\overline{A} - 3(\overline{A})^2}{4(1 - \overline{A})}, \tag{25}$$

$$E(D_{i,j}) = \frac{4 - 3\overline{A}}{4(1 - \overline{A})}, \tag{26}$$

where $2 \leq i \leq log_2 N$, $1 \leq j \leq N$.

Thus, the total delay $E(D)$ experienced by an incoming cell is given by:

$$E(D) = \frac{2\overline{A} + 2\overline{A^2} - 3(\overline{A})^2}{4\overline{A}(1 - \overline{A})} + (log_2 N - 1)\frac{4 - 3\overline{A}}{4(1 - \overline{A})} \tag{27}$$

Remark:

The general result given in eq. (27) coincides with the result reported in [12] when we specialize our result to the Bernoulli arrival case which was considered in [12].

4. Numerical results

The analytical results obtained in the previous section will now be examined numerically. Based on the expression of eq. (27), the total delay was computed for different arrival processes and different switch sizes. The results are shown in fig. 3. Three different arrival processes were assumed: Bernoulli, binomial and Poisson. The switch size is 16×16 in the first plot and 64×64 in the

second one. From this figure, it can be said that the performance of the three processes is nearly the same for light loads. However, there is an observed difference in the heavy traffic case.

To assess the infinite queues assumption employed in the present analysis, we plot in fig. 4 the (maximum) expected queue length as given by eq. (22). It is noted that for the three considered arrival processes the expected queue length at the first stage (eq. 22) is greater than or equal to the expected queue length at the other stages (eq. 25), i.e., $E(X_{1,j}) \geq E(X_{i,j})$, $2 \leq i \leq log_2 N$, $1 \leq j \leq N$. Therefore, we use eq. (22) to compute the maximum occupation. Moreover, it is noted that the given expressions for occupation are independent of the switch size. From fig. 4, we see that the expected queue length doesn't exceed a small finite value for almost all the working loads. Thus, in the practical implementation a small finite queue size will be sufficient. In addition, the queues at stages following the first one can assume smaller sizes.

To make this point more clear, we simulate the ATM switch operating with a finite queues size (*L*) and compute the cell loss probability.

The results are shown in fig. 5 (*N* = 4). In the light load case, the cell loss probability is almost zero for all the studied queue sizes. For the heavy traffic case, a choice *L* = 8 keeps this probability less than 0.02 in the Bernoulli case and less than 0.06 in the Poisson case. Larger queue sizes may be considered to obtain smaller cell loss probability.

5. Conclusions

Banyan network based ATM switches were analyzed using a discrete time queueing system model. General arrival stream and uniform traffic were assumed. The switch was assumed to have internal output queues of infinite size. Analytical expressions for three performance measures (utilization, occupation and delay) were computed to add new general results compared with the existing ones in the literature [12]. Moreover, the infinite queue size assumption was assessed by computing (using simulation) the cell loss probability for switches with finite queue size. It was shown that a small cell loss probability can be achieved with a small queue size. This is an important result from a practical point of view.
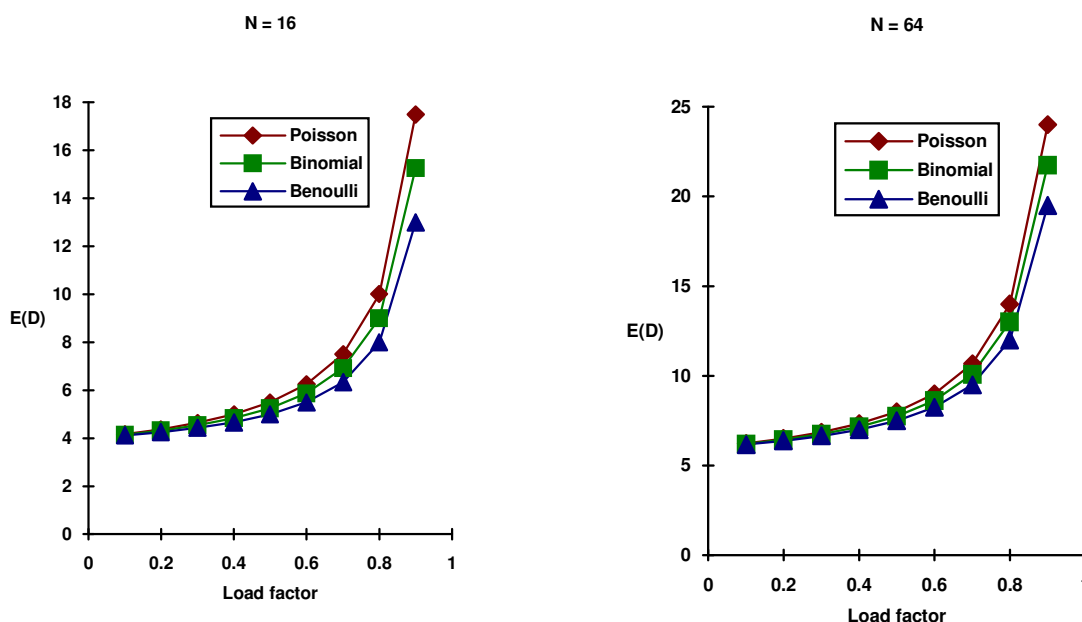
N = 16

N = 64
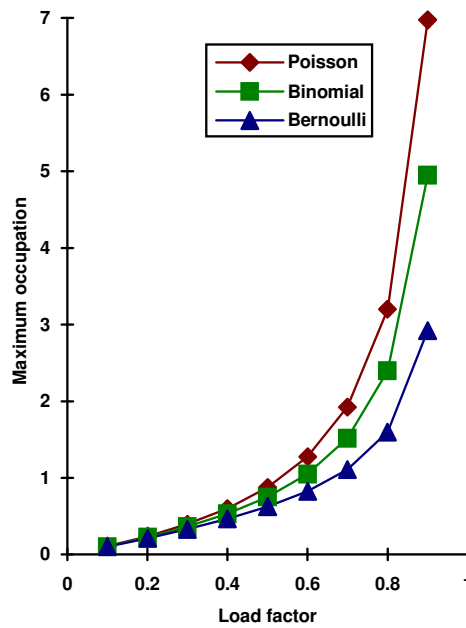

Fig. 3. Total delay for different arrival streams and switch sizes.

Fig. 4. Maximum occupation for different arrival streams.

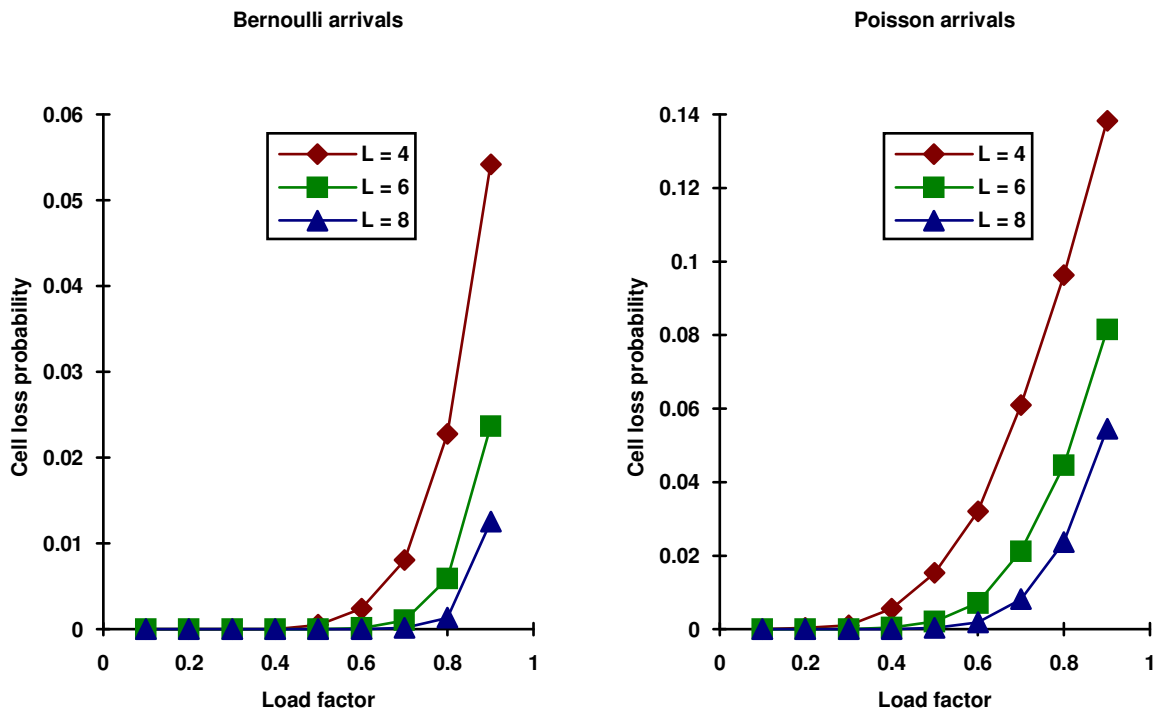**Bernoulli arrivals**   **Poisson arrivals**

Fig. 5. Cell loss probability for different arrival streams and buffer sizes.

The non-uniform traffic assumption may be more realistic. Hence, the aim of our next paper is to analyze the present model working under a non-uniform traffic pattern. Moreover, banyan network based ATM switches have several performance enhancement techniques (see for example: [8-11], besides the internal output queueing employed here. Examining

ATM switches provided with some of these performance enhancement techniques needs a separate study and is expected to appear in an incoming paper.

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