An integrated CMOS Golay decoder

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A novel CMOS VLSI architecture of a Golay decoder is presented for the implementation of a (23,12) Golay code. The proposed architecture is based on a novel Golay decoder relationship between the syndrome and the error patterns. It has the advantage of reducing the number of logic gates needed to implement the look up table over the previous implementations. This in turn leads to significant area saving for on-chip storage, reduction in power consumption and speeding up the correction process compared to the conventional decoding approaches.

يستعرض هذا البحث تصميمًا مبتكرًا لدائرة متكاملة متناهية الصغر تستخدم في تشفير الإشارات بنظام "Golay" باستخدام تقنية CMOS تعتمد على علاقة مبتكرة بين منوال الأخطاء بالإشارة وبين مجموعة مما أعراضها يقلل حجم الدوائر الإلكترونية المتناهية الصغر اللازمة للتخزين وتقليل الطاقة المستهلكة والسرعة العالية في تصحيح الإشارة مقارنة بطرق التشفير المعروفة.

Keywords: Block codes, Golay decoder, Syndromes, Error patterns

1. Introduction

Channel coding is one of the most important factors that affects the design of any communication system [1,2]. The (23,12) Golay code which is one of the linear block codes class is a binary code that is capable of correcting any combination of three or fewer random errors in a block of 23 bits. The 23 bits message is generated from a 12 bit input information at the transmitter by adding 11 redundant bits. Fig. 1 shows the flow chart of the ordinary decoding procedure. The decoding steps start by calculating the syndrome and saving the 23 bits received message since it will be used in the correction stage, then the calculated syndrome is used to find the suitable error pattern from the look up table. The selected error pattern together with the saved message are used to find the position of the error and correct it [3,4].

The new design implements the Golay (23,12) decoder by modifying the decoding procedure shown in fig. 1. In the novel design the look up table has been divided into two parts according to a relationship between the calculated syndrome and the error patterns. The two parts of the look up table work concurrently resulting in reducing the number of logic gates used to implement the look up table.

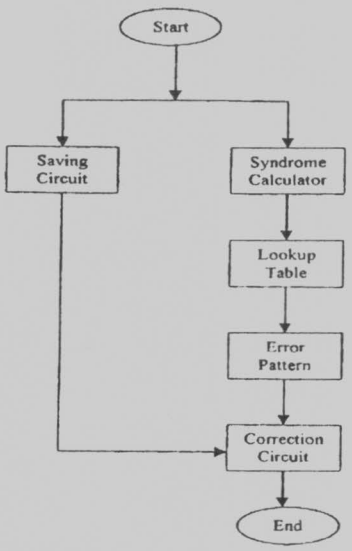

Fig. 1. The flow chart of ordinary decoding process.

The new decoder is based on a novel relationship between the syndromes and the error patterns, resulting in an improvement in the implementation of the look up table consequently reducing the number of logic gates needed and speeding up the correction capability of the decoder.

By carefully investigating the syndromes for all possible errors it is found that some of syndromes look like the corresponding error

pattern whereas others are different. Therefore, the syndromes that are related to the error pattern can be used for correction process whereas the unrelated syndromes can be saved in the look up table. Fig. 2 shows the flow chart of the new decoding process. The calculated syndrome is weighted using the weighting circuit to decide whether it will be used for correcting the input or it will be used for selecting the corresponding error pattern from the look up table module.

The new system has been implemented using Alliance Cad Tools.

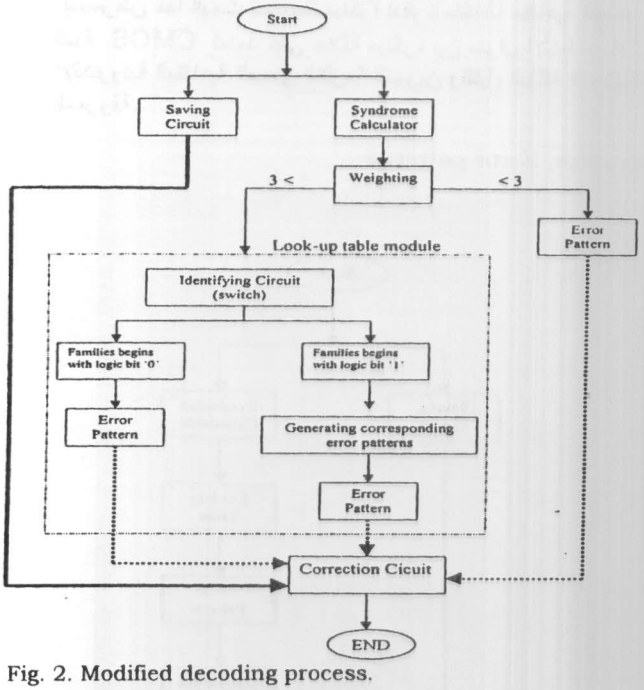

Fig. 2. Modified decoding process.

2. Theory of Golay codes

2.1. The generator polynomial for (23,12) Golay codes

The generator polynomial of the Golay code is given either by eq. (1) or eq. (2) [4, 5],

$$G(X)= X^{11}+X^9+X^7+X^6+X^5+X+1, \quad (1)$$

$$G(X) = X^{11}+X^{10}+X^6+X^5+X^4+X+1. \quad (2)$$

The number of correctable errors t in Golay code is given by,

$$t = [0.5(d_{min}-1)] , \quad (3)$$

where, d_{min} is the minimum distance of the code.

For a Golay code d_{min} is equals to 7 [4, 5], this leads to t=[0.5(7-1)]=3 detectable and correctable errors.

2.2. Decoding procedure in Golay codes

The decoding process of Golay codes starts with calculating the syndrome S which is given by [5]

$$S= YH^T . \quad (4)$$

Where;
H^T is the parity check matrix.
Y is the received vector.

The calculated syndrome is used to find the most probable error pattern Z from the look up table. The look up table is the storage of all error patterns. In order to correct the errors in the received vector, the error pattern is added (i.e modulo 2 addition) to the received vector to obtain the most probable code word X. Eq. (5) gives the relation between the corrected output X, the received vector Y and the error pattern Z.

$$X= Y \oplus Z . \quad (5)$$

When the code is cyclic the syndrome computation is performed by shift registers similar to those used for encoding [4, 5].

3. The Golay decoder system

Fig. 3 shows the block diagram of the proposed Golay decoder. It consists of a syndrome calculator, a saving circuit, a look up table and a correction circuit. The syndrome calculator calculates the syndrome using the 23 bit input message. Meanwhile, the input message is saved in the saving circuit. The calculated syndrome is used to generate the error pattern from the look up table. The final stage is the correction circuit which finds the error position in the received message and correct it by XORing the saved message with the error pattern.

3.1. The syndrome calculator

Fig. 4 shows the circuit diagram of the syndrome calculator and its layout. It is responsible for generating the syndrome using the received input bits. The calculated syndrome is required to select the corresponding error pattern from the look up table.

The syndrome calculator consists of 11 shift register connected in series and 6 XOR gates (module 2 addition) required for implementing the generator polynomial.

3.2. The saving circuit

It is responsible for saving the input received message to be provided to the correction circuit. It serves as a delay unit that delays the received message until it reaches the correction. Fig. 5 shows the circuit diagram of the saving circuit and its layout, it consists of a cascaded 24 D-flip flops (shift registers) to save a 23 bit input message, the first D-flip flop is used to synchronize the rest of D- flip flops.

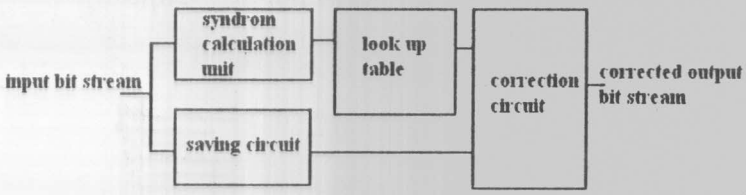

Fig. 3. The block diagram of the proposed decoder.

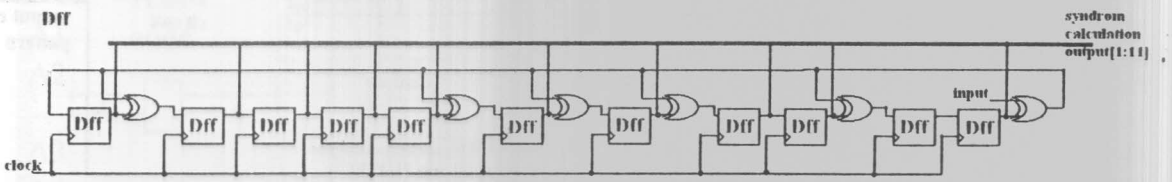

Fig. 4-a. The syndrome calculator circuit.

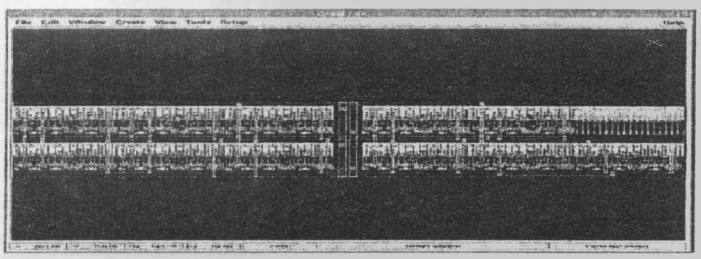

Fig. 4-b. The layout of the syndrome calculator circuit.

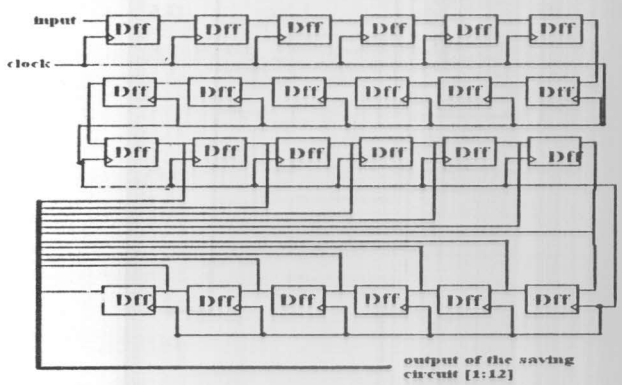

Fig. 5-a. The saving circuit.

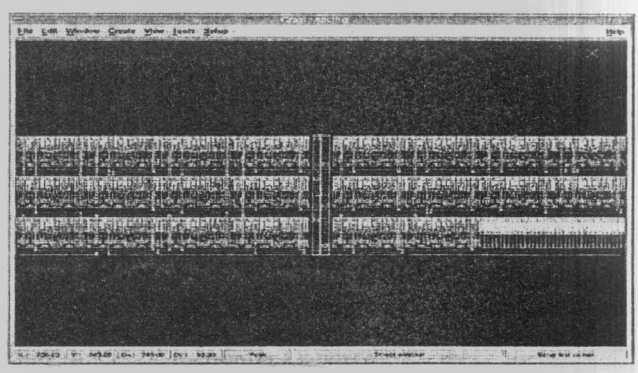

Fig. 5-b. The layout of the saving circuit.

3.3.The look up table

It is used to relate the calculated syndrome with the corresponding error pattern that detects the position of the error in the received message. In the new system that implements the Golay (23,12) code, the received message consists of 23 bits; 12 bits for the original message and 11 bits for parity. Hence, the number of syndromes needed to be inserted in the look up table is 2^{11} (2048 syndromes) which results in a very large look up table and hence a very large Si area to be implemented.

The novel design of the look up table is based on a relationship between the calculated syndrome and the error patterns which results in reducing the size of the look up table.

By carefully studying the syndromes for all possible errors it is found that:

1- If errors occur in the first 11 bits of the input received message, the syndrome will be like the error pattern.

2- If errors occur after the 11^{th} bit this will generate syndromes that contain more than three bits having logic "1" and it will be different from the error pattern. Hence, this group of error patterns have to be saved in the look up table with its syndromes.

The look up table consists of a pattern generating circuit and a set of OR gates.

The pattern generating circuit is responsible for generating the error pattern which corresponds to the input calculated syndrome, this is achieved by XORing the input syndrome with a set of logic '0' and logic '1' connected as shown in fig. 6. The outputs of the XOR's are weighted using weighting circuit which is responsible for enabling a set of AND gates at the output stage of the pattern generating circuit. The circuit diagram of the pattern generating circuit and its layout is shown in figs. 7-a and 7-b, respectively.

Figs. 8-a and 8-b show the circuit diagram of the weighting circuit and its layout, respectively. It sums the syndrome bits to generate the enabling signal. It consists of six half adders and five 4 -bit full adders.

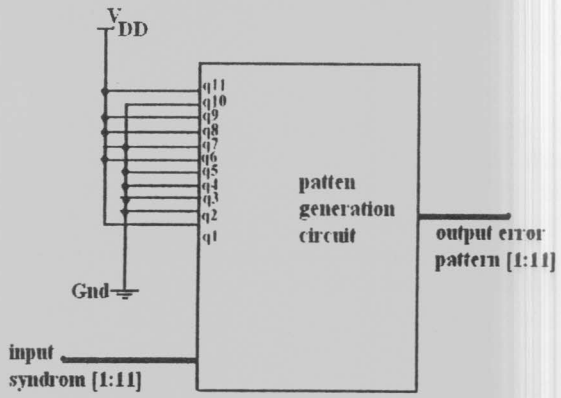

Fig. 6. The block diagram of the pattern generating circuit.

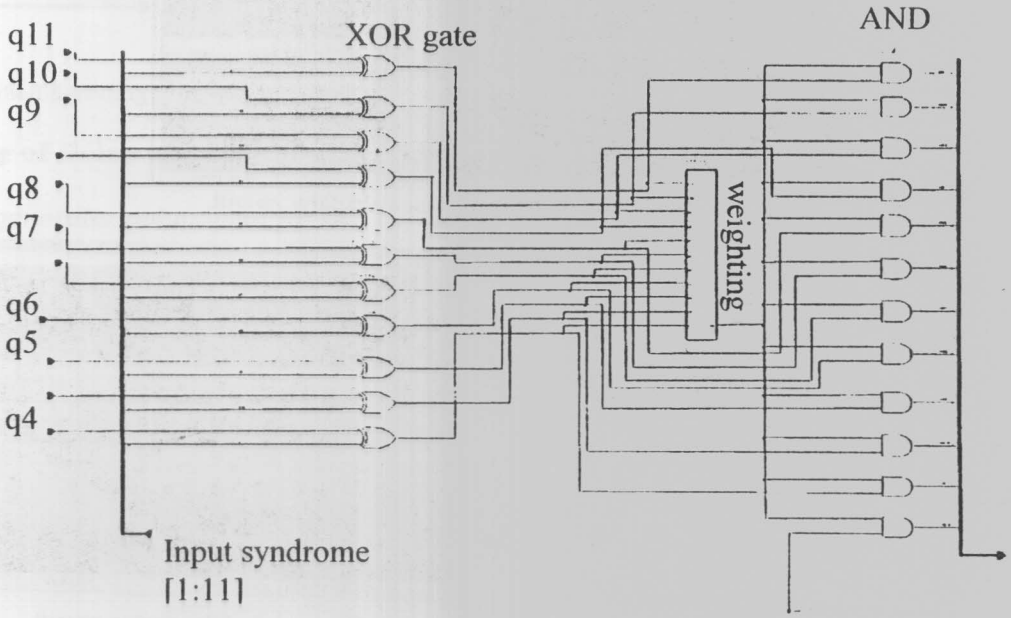

Fig. 7-a. The pattern generating circuit.

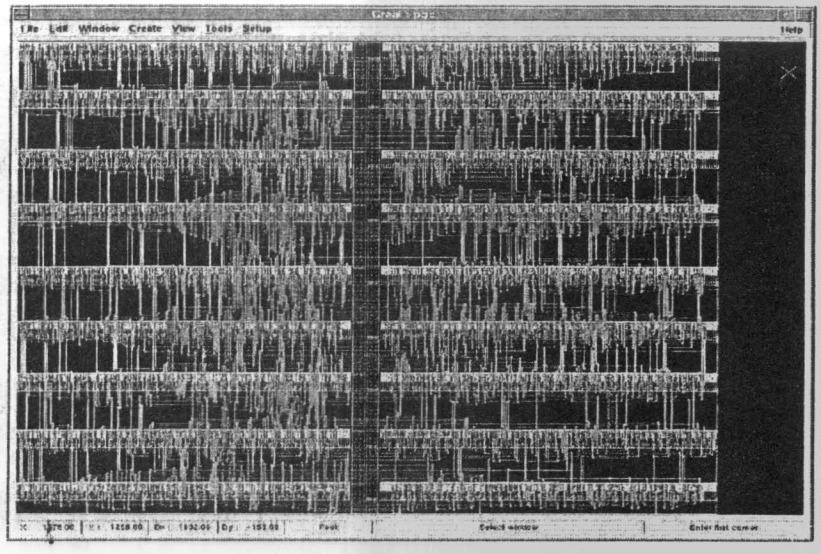

Fig. 7-b. The layout of the pattern generating circuit.

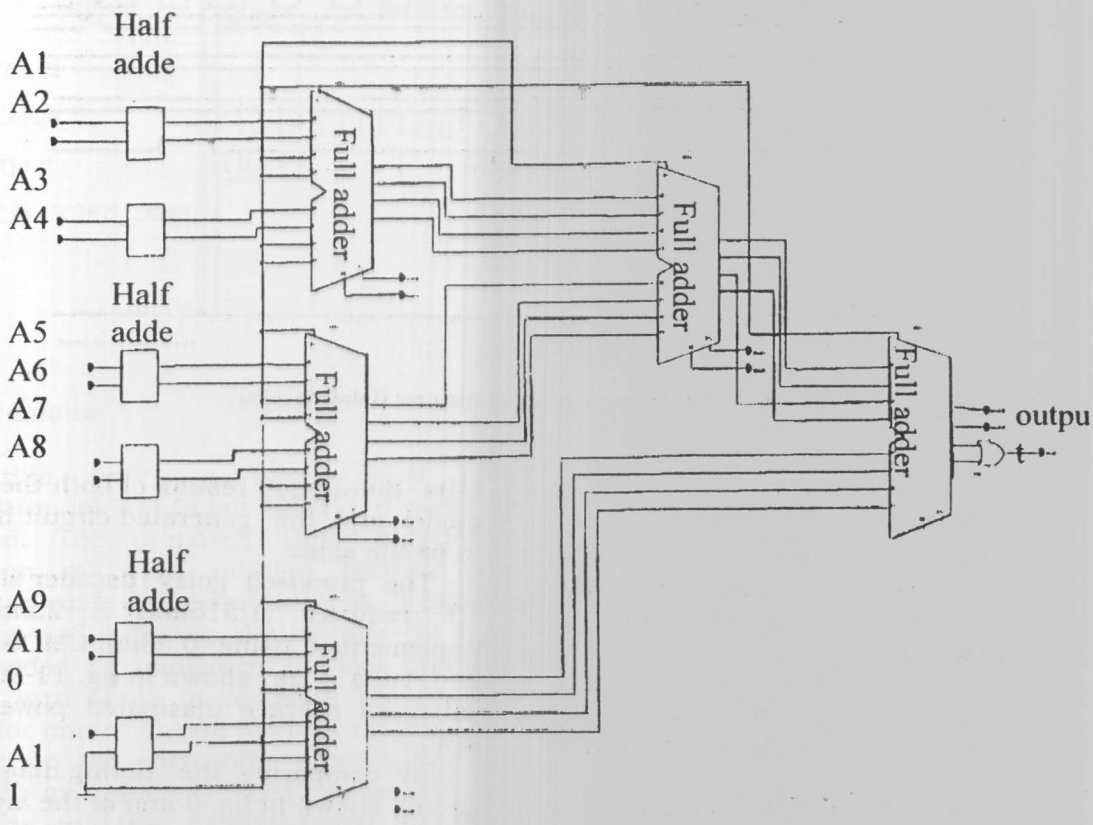

Fig. 8-a. The weighting circuit.

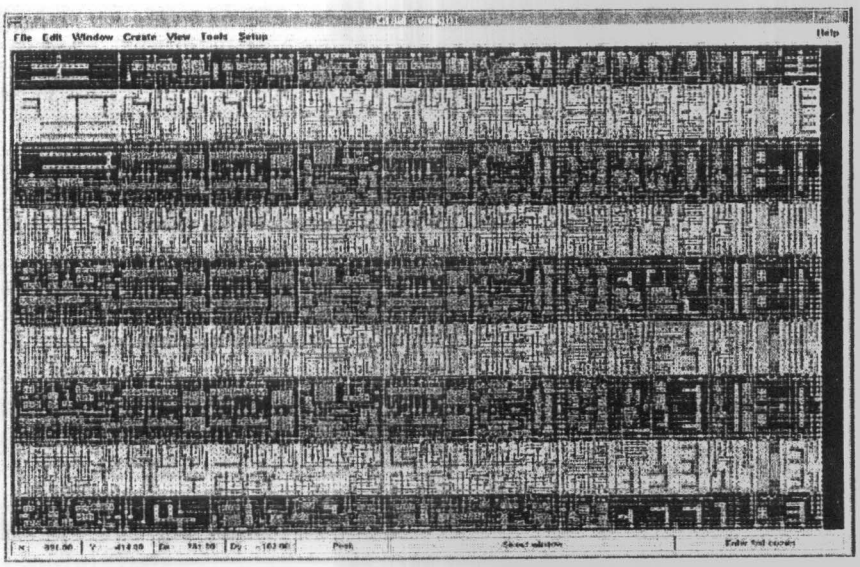

Fig. 8-b. The layout of the weighting circuit.

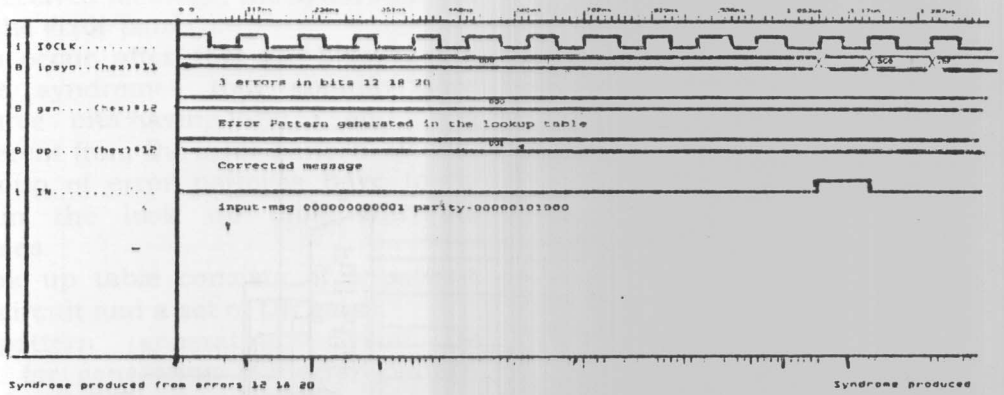

Fig. 9. The timing diagram of the new Golay decoder.

3.4. The correction circuit

It is the final stage in the decoding process where the saved received message is compared with the generated error pattern to produce the corrected message.

The correction circuit compares every bit in the saved message with the adjacent bit in the error pattern and realized using XOR gates.

The proposed Golay decoder has been designed by generating and synthesizing the VHDL code of the behavioral model from which the layout is generated.

Fig. 9 shows the timing diagram of the novel Golay decoder system which runs at 56 MHz. Simulation results of both the behavioral model and the generated circuit have proven to be the same.

The proposed golay decoder shown in fig. 10 requires (1.516mm X 2.2mm) to be implemented using 0.25μm CMOS technology and runs - as shown in fig. 11- at 55.3 MHz with an average dissipated power of 1.475 mW.

By comparing the timing diagrams of the circuit shown in fig. 9 and of the layout shown in fig. 11, it is clear that both simulation results are almost identical except for the slight delay (2.26 ns) in the generated layout which is due to the parasitic and interconnects in the layout [6].

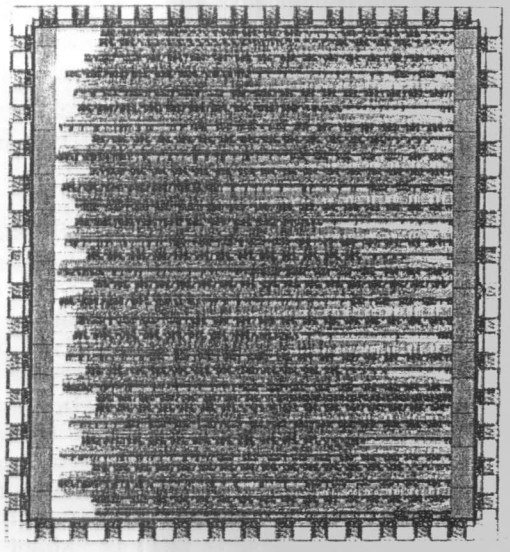

Fig. 10. The layout of the novel Golay decoder.

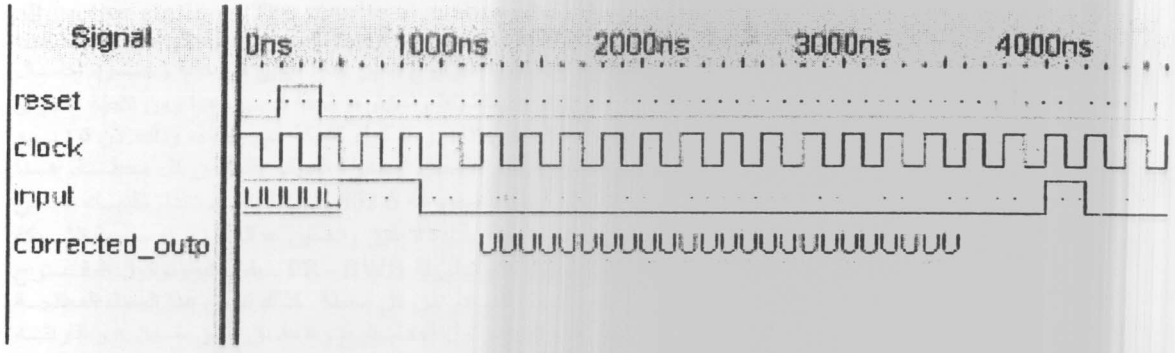

Fig. 11. The timing diagram of the layout.

4. Conclusions

In this paper a new CMOS chip architecture of a Golay (23,12) decoder is presented. The proposed Golay decoder is based on a new relation between the syndromes and the error patterns. It has the advantage of reducing the number of logic gates needed to implement the look up table. This in turn leads to reducing the Si area needed for implementing the look up table and speeding up the correction process. The end result is an efficient VLSI implementation compared to the conventional decoding approaches.

References

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