Impact of the statistical nature of physical parameters on short and narrow channel MOSFETs

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A 3-D electrostatic model for short and narrow channel MOSFETs is presented. The model is based on a numerical solution of Poisson's equation using the finite difference approximation technique. The model is applied to the case of electrically stressed LDD devices where hot-carrier induced interface traps are present. The impact of the statistical nature of such traps and other physical parameters on the static characteristics of short and narrow channel devices operating in the ohmic region is extensively studied. The simulation results have shown that for submicron devices, the spread in the channel conductance and transconductance due to such a statistical nature is quite significant especially in subthreshold.

يقدم البحث نموذجا الكتروستاتيكيا ثلاثيا الأبعاد للترانزيستورات (معدن-أكسيد-شبه موصل) ذات القنوات القصيرة والضيقة آخذا فى الأعتبار الطبيعة الأحصائية للبرامترات الفيزيائية لهذه النبائط. وقد طبق هذا النموذج على نبائط ذات مصرف منخفض التشـــويب ومعرضة لاجهادات كهربية. وقد تم دراسة تأثير مصايد السطح البينى المستحثة من الألكترونات الساخنة (ذات الطاقة العالية) كما تم دراسة صدى الطبيعة الاحصائية للبرامترات الفيزيائية على الخواص الاستاتيكية لهذه النبائط. وقد أظهرت نتائج المحاكـــاة مـدى التناثر الشديد فى كل من خواص الموصلية والموصلية المحولة فى حالة النبائط ذات القنوات شـــديدة القصـــر والضيـــق (كســور الميكرومتر) بسبب هذه الطبيعة الاحصائية مما يؤثر بدوره على أداء الدوائر المتكاملة عالية الكثافة والمحتوية على هذه النبائط وكذا ظهور مشاكل الاعتمادية وعدم التماثل.

Keywords: 3-D electrostatic model, Short/narrow channel MOSFET, Physical parameter statistics.

1. Introduction

As the dimensions of MOSFETs and related devices in VLSI circuits continue to shrink, several reliability problems may evolve [1]. One of these problems is the impact of the statistical nature of different physical parameters on the device static and dynamic performances. Physical parameters such as substrate doping, source/drain doping profiles and gate oxide thickness suffer from spatial variations throughout the processed wafer depending on the technology employed. Moreover, in short channel devices, hot-carriers may result in locally damaged drain regions where induced interface and oxide traps are created. These traps have also statistical spatial and energy distributions. As a result of this statistical nature and due to the huge number of devices in VLSI chips, yield and reliability degradations are certainly expected. In order to investigate accurately how the statistical nature of different physical parameters affects the device behavior, three-dimensional (3-D) modeling is required.

In this paper, a 3-D electrostatic model for electrically stressed lightly doped drain (LDD)-MOSFETs is presented. The model takes into account all the device details including the exact doping profiles and the statistical nature of different physical parameters. Potential and charge distributions within the device in all operating regimes (subthreshold and strong inversion) are extensively studied. The model results in the channel conductance and transconductance in the ohmic region as a function of the gate voltage in all operating regimes.

2. Model presentation

The model relies on the solution of Poisson's equation using the seven-point finite difference approximation in a network of nodes within the device boundaries [2]. The grid structure chosen for such a technique is

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a non-uniform spacing 3-D rectangular mesh with enhanced number of nodes in the regions where the structure details is of great importance (channel and LDD regions). The discrete approximation to Poisson's equation results in a system of non-linear equations, which is solved using Newton-Successive-Linear-Over-Relaxation (NSLOR) iteration technique [3,4] to obtain the potential and charge distributions throughout the grid structure.

The doping profiles in the source, drain and LDD regions and also in the implanted layer in the channel region (used for threshold voltage adjustment) are modeled using Gaussian distributions. Lateral diffusions in the overlapped regions between source/drain and LDD's and underneath the gate oxide are also incorporated in the model. The spatial and energy distribution of the hot-carrier induced interface traps is introduced in the model. These traps are localized in the non-overlapped LDD region where the electric field is high [5].

Now, if we assume that some physical parameters such as the induced interface traps, gate oxide thickness and doping profiles vary randomly within the device, surface potential and free carrier density fluctuations may result. To express this quantitatively, we divide the 3-D grid structure into small characteristic volumes over which the physical parameter of interest varies with a probability density function of the form [6]

$$P(X) = \frac{1}{\sqrt{2\pi}\,\sigma_X} \exp\left(- \frac{(X - \overline{X})^2}{2\sigma_X^2} \right), \tag{1}$$

where X and $\overline{X}$ denote the value of the physical parameter under consideration and its mean value, respectively, and σ_X is the standard deviation of the distribution.

The surface potential and free carrier fluctuations may affect the dc and ac behaviors of the device. The dc behavior comprises the channel conductance and transconductance characteristics at different biasing conditions. The ac behavior deals with the capacitance and conductance characteristics when a small ac signal with different frequencies is superimposed on the gate bias. The latter case has been extensively studied and published elsewhere [2].

In the next section, we investigate the impact of the statistical nature of physical parameters on the spread in the channel conductance and transconductance characteristics of short and narrow channel devices operating in the ohmic region. In this region of operation, it is assumed that the application of small values of drain voltage ($\leq$ 0.1 V) does not disturb significantly the inversion charge distribution along the channel. Therefore, the channel conductance G_{DS} as a function of the applied gate voltage V_{GS} can be simply expressed as

$$G_{DS}(V_{GS}) = q\int_0^W \left[\int_0^L \left(\int_0^\infty \mu_n(x,y,z)\, n(x,y,z)\, dy \right)^{-1} dx \right]^{-1} dz, \tag{2}$$

where x, y and z represent the coordinates in the channel length direction, normal to the Si-SiO_2 interface and in the channel width direction, respectively, L is the channel length, W is the channel width, $n(x,y,z)$ is the free carrier density obtained from the 3-D solution of Poisson's equation and μ_n is the electron mobility, which can be expressed as [7]

$$\mu_n = \frac{\mu_o}{1 + \dfrac{E_{eff}}{E_c}}, \text{ with, } \mu_o = \frac{\mu_{oo}}{1 + \alpha(Q_f + q D_{it})} \text{ and } E_{eff} = \frac{1}{\varepsilon_{si}}\left[Q_D + \frac{Q_i}{2} \right], \tag{3}$$

where μ_o is the low field mobility, E_{eff} is the effective transversal electric field across the channel, E_c is the critical electric field, μ_{oo} and α are functions of doping concentration. The quantities Q_f, Q_D and Q_i are the fixed oxide charge, the depletion layer charge, and the inversion layer charge density, respectively.

The transconductance $g(V_{GS})$ normalized with respect to the drain-source voltage is simply given by [4]

$$g(V_{GS}) = \frac{\delta G_{DS}}{\delta V_{GS}} . \quad (4)$$

For simplicity, we will shortly refer to $g(V_{GS})$ as the transconductance.

3. Results and discussion

The physical parameters (except the channel width) of the device under consideration and which are used in the simulations, are taken comparable to those of electrically stressed LDD-MOSFETs whose experimental data were recently published [5,8]. These parameters among other model parameters are summarized in Table 1. The effective channel length is taken equal to 0.65 μm, while the channel width is varied in the range between 1 μm and 50 μm. The standard deviation of the statistical distribution of the physical parameter of interest is varied in the range between 0.05 and 0.1 of the parameter's mean value.

Fig. 1. shows the surface potential distributions along the channel (coordinate x) at different positions in the interface plane (xz-plane), when incorporating the statistical distributions of different physical parameters. The characteristic volumes chosen in this simulation are cubes of 0.05 μm edge (about half of the depletion layer width in the substrate). The statistical spatial distribution of the hot-carrier induced interface trap density D_{it} used in the simulation is shown in fig. 2. It is noted that the surface potential fluctuations are relatively large in subthreshold (V_{GS} = 0.4 V) and negligibly small in strong inversion (V_{GS} = 2 V). It is also noted that for a given value of V_{GS}, the surface potential is not uniform along the channel and its values in the source- and drain-end regions are not symmetric. This is attributed to the 2-D nature of the channel, which results from the presence of the source- and drain-substrate junctions in close proximity and also due to the asymmetric spatial and energy distribution of the induced interface traps. The interface trap density is maximal in the LDD region and decreases monotonically when approaching the source. If we consider acceptor-like interface traps, they contribute to a negative charge when occupied by electrons. This will decrease the values of the surface potential near the drain in comparison with its values near the source. The modeling of the surface potential in such a manner will result in an accurate modeling of the channel conductance G_{DS} in all operating regimes. fig. 3 and 4. show the simulation results of $G_{DS}(V_{GS})$ and $g(V_{GS})$ with the channel width W as a parameter. It is interesting to note that for short and narrow ($\leq$ 1 μm) channel devices, the spread in the channel conductance and transconductance is quite significant, especially in subthreshold. As the channel width increases, the spread decreases monotonically and becomes negligibly small for channel widths greater than about 10 μm. This is expected since for relatively wide devices, the number of the characteristic volumes becomes quite large, which causes the statistical distribution of any variable (surface potential, for example) along the channel width to be independent of W. In this case, the effect of the physical parameter statistics is negligible and a 2-D modeling is quite sufficient.

The above result is very important since it reflects the impact of the statistical nature of physical parameters on the performance of short and narrow channel devices operating in subthreshold. Such a case is commonly encountered in VLSI circuits where minimum feature size devices are used to save the chip area and subthreshold operation is recommended to decrease the power consumption. Therefore, one expects non-negligible mismatch and reliability problems in such circuits due to this statistical nature.

4. Conclusions

We have presented a 3-D electrostatic model for short and narrow channel MOSFETs taking into account the statistical nature of different physical parameters. The most important interesting result is that this statistical nature affects significantly the static behavior of these devices especially in subthreshold and may certainly create reliability problems in VLSI circuits. This suggests also that more accurate CAD models, which take into account such a phenomenon, have to be employed.

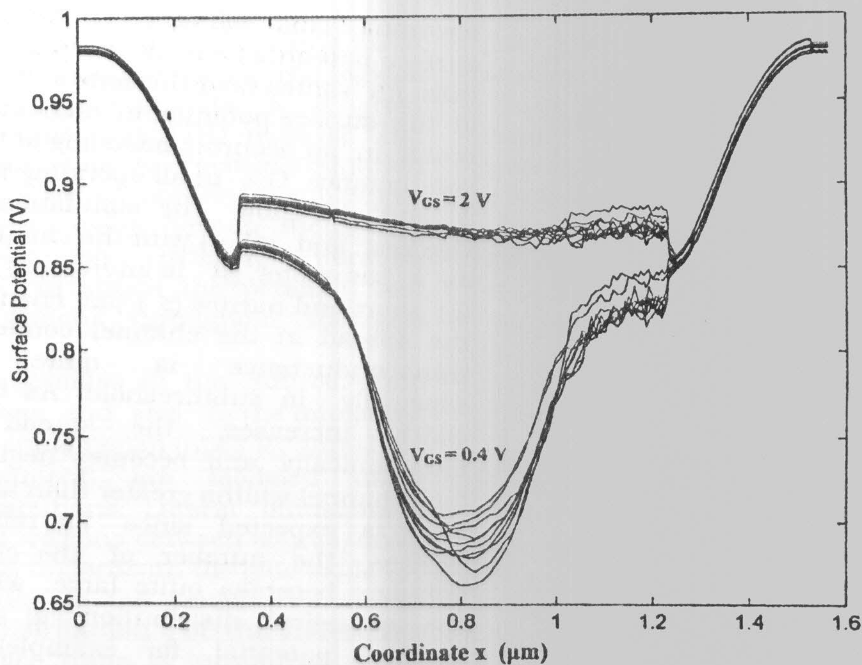

Fig. 1. Surface potential distributions along the channel in the interface plane in subthreshold (V_{GS}=0.4 V) and strong inversion (V_{GS}=2 V) regimes.

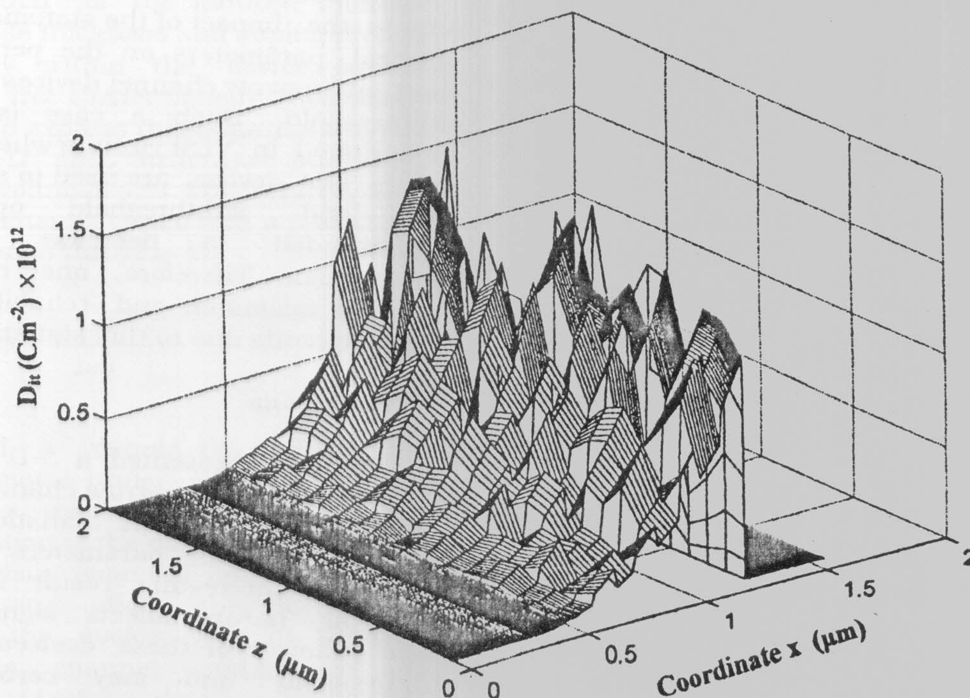

Fig. 2. Statistical spatial distribution of the hot-carrier induced interface trap density used in the simulations of fig. (1).

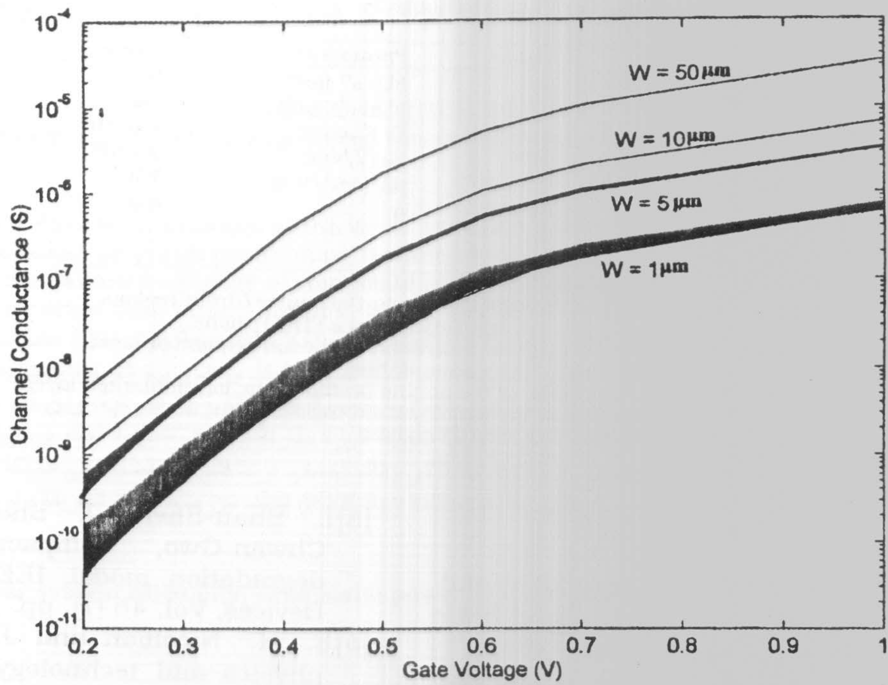

Fig. 3. Channel conductance versus gate voltage with the channel width as a parameter.

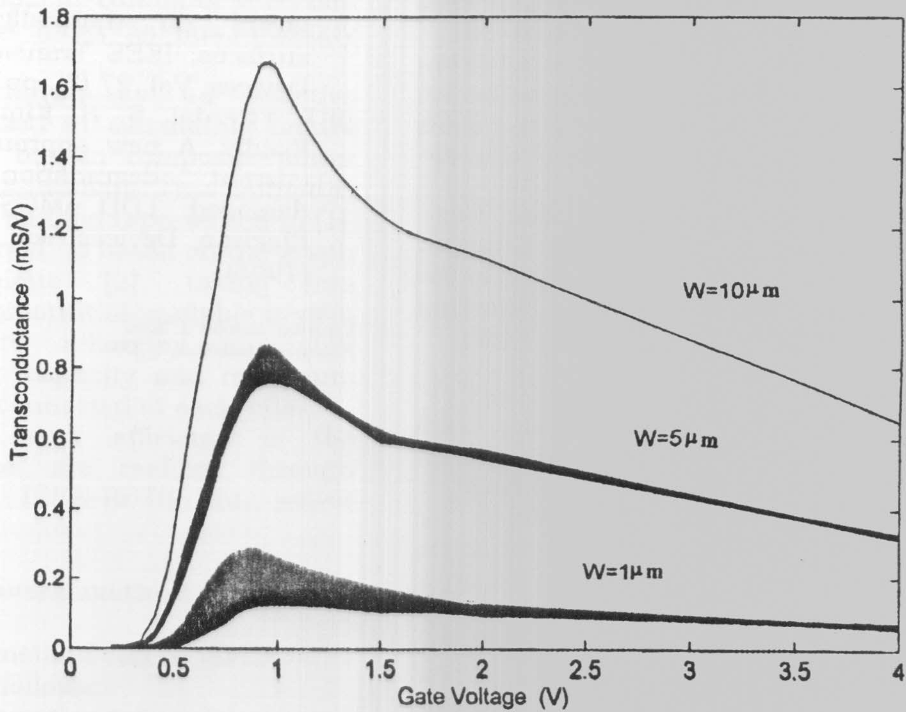

Fig. 4. Normalized transconductance versus gate voltage with the channel width as a parameter.

Table 1
Device physical and model parameters

Parameter	Value	Parameter	Value
d_{ox} (A°)	160	$(d_j)_{S,D}$*7 (μm)	0.3
L_{eff} (μm)	0.65	$(d_j)_{LDD}$*8 (μm)	0.2
N_a*1 (cm^{-3})	6.2×10^{16}	Q_f ($C.cm^{-2}$)	1.6×10^{-9}
$(N_{DS})_{S,D}$*2 (cm^{-3})	10^{20}	E_c (V/cm)	2×10^{5}
$(N_{DS})_{LDD}$*3 (cm^{-3})	6.5×10^{17}	μ_{oo} (cm^2/V.s)	750
N_{AP}*4 (cm^{-3})	8×10^{17}	α	0.2
Y_p*5 (μm)	0.02		
σ_I*6 (μm)	0.06		

*1. Substrate doping.
*2. Maximum donor concentration in the source/drain regions.
*3. Maximum donor concentration in the LDD regions.
*4. Maximum acceptor concentration in the ion-implanted layer.
*5. Projected range of the ion-implanted layer.
*6. Standard deviation of the doping profile in the ion-implanted layer.
*7. Junction depth of the source/drain regions.
*8. Junction depth of the LDD regions.

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