A 3-D electrostatic model for short channel MOSFETs: application to split-admittance technique

M. EL-Sayed, and N. Salah
Electrical Engineering Department, Alexandria University, Alexandria, Egypt

An efficient 3-D electrostatic model for short channel MOSFETs has been presented. The model is based on the numerical solution of Poisson equation using the seven-point finite difference approximation. The model takes into account all device details including statistical nature of physical parameters such as substrate doping, gate oxide thickness, and interface trap density. Potential and charge distributions within the device in all operating regimes have been extensively studied. An accurate small-signal transmission-line model, whose components are evaluated from the proposed 3-D model, has been also presented. The small-signal model has been implemented in a circuit simulator (SPICE) and applied to the case of the recently proposed split-admittance technique. Comparisons between the simulation results and the experimental results have been carried out, and assumptions employed in the conductance and conductance-based techniques have been thoroughly studied and criticized.

يقدم البحث نموذج الكتروستاتيكى ثلاثى الأبعاد ذو كفاءة عالية للترانزيستورات (معدن-أكسيد-شبه موصل) ذات قنوات التوصيل القصيرة. ويعتمد هذا النموذج على حل عددى لمعادلة بواسون باستخدام طريقة الفروق المحددة ذات السبعة نقاط. ويأخذ هذا النموذج فى الاعتبار جميع التفاصيل الدقيقة لبناء الترانزيستور وكذا الطبيعة العشوائية لبعض برامترات الترانزيستور. هذا ويمكن النموذج من الحصول على توزيعات ثلاثية الأبعاد للجهود والشحنات داخل جسم الترانزيستور فى مختلف ظروف التشغيل. كما يقدم البحث نموذج دقيق للاشارات الصغيرة للترانزيستور يعتمد على نموذج خطوط النقل الموزعة غير المنتظمة وذلك لدراسة الأداء الديناميكى للترانزيستور عند تطبيق اشارات صغيرة مترددة على جهد انحياز ثابت على البوابة. وقد استخدم النموذج الالكتروستاتيكى ثلاثى الأبعاد السابق ذكره فى حساب جميع مكونات نموذج الاشارات الصغيرة المقترح وتم محاكاة هذا النموذج باستخدام برنامج محاكاة للدوائر الكهربية والالكترونية (SPICE). ولدراسة كفاءة النموذجين المقترحين فقد تم مقارنة النتائج النظرية الحاصل عليها من المحاكاة بنتائج معملية نشرت سابقا لتقنية المسامحة المشطورة فى هذا النوع من النبائط شبه الموصلة. هذا وقد مكنت نتائج المقارنات من مناقشة ونقد الفروض والتقريبات المستخدمة فى التقنية المذكورة كما أوضحت الحاجة الملحة لاستعمال نماذج الكتروستاتيكية وديناميكية دقيقة لدراسة هذا النوع من النبائط.

Keywords: 3-D electrostatic model, short-channel MOSFET, Split admittance.

1. Introduction

The increasing emphasis on VLSI (Very Large Scale Integration) is presenting a challenge in the area of device design [1]. The design of these devices requires reducing the area and power dissipation. The problem of design and process control can be aided by the use of accurate device models [2]. The accurate analysis of devices of complex structures requires 2-D (Two-Dimensional) and 3-D (Three-Dimensional) numerical solutions, which can be applied to the investigation of many device characteristics, and emerges as a powerful engineering tool which can guide fabrication process development.

Whereas, feature sizes of MOSFETs are aggressively scaled down, hot carriers generated by the large electric fields in the drain region appears to be an important parasitic effect for such devices even under normal operating conditions [3,4]. Energetic carriers may surmount the Si-SiO_2 energy barrier and be trapped within the gate oxide layer or generate interface traps. Also, with increasing advancements in the VLSI technologies such as ion implantation, electron beam and x-ray lithography and plasma etching, damage at the Si-SiO_2 interface may be created [5]. In the literature, several experimental techniques were

proposed and studied in great detail for interface trap characterization in MOSFETs. The well-known examples, which can yield quantitative information concerning the interface trap properties, are charge pumping [6,7], split-current [8], conductance [9] and conductance-based techniques. The latter includes the transfer admittance [10] and the split-admittance [11] methods. Although the conductance and conductance-based techniques have been successfully applied to relatively short channel devices, they suffer from limitations due to approximations employed in treating the channel time constant and the interface trap distribution along the channel. The channel time constant has been always neglected in the operating frequency range (up to several MHz) employed in the measurements. The interface traps are assumed uniformly distributed along the channel and when a statistical trap distribution is considered, it is treated in a simplified manner. These methods have also neglected the two-dimensional nature of the channel near the source and drain ends. These oversimplified assumptions have led to the use of a lumped-element small-signal model to analyze the device conductance and capacitance characteristics. In order to study such two-dimensional effects, a more accurate small-signal model such as a distributed TL (Transmission Line) model has to be used. This model permits also to study the statistical nature of different physical parameters such as interface trap density, substrate doping and gate oxide thickness. The evaluation of the circuit elements of the TL model in such a case necessitates the development of a numerical 3-D model for the device under consideration.

In this paper, a 3-D electrostatic model based on the solution of Poisson's equation in short channel MOSFETs using the seven-point finite difference approximation is presented. The model considers all the device details including the exact doping profiles and the statistical nature of different physical parameters. The model has been used to investigate the dynamic behavior of the device under the application of a small-signal gate voltage of different frequencies in different biasing regimes. The device split-admittance has been analyzed using a small-signal TL model with the aid of a circuit simulator (SPICE). The model results have been compared with recently published split-admittance measurements, carried out on electrically stressed device [11]. The assumptions and approximations employed in the conductance and conductance-based techniques have been then discussed and criticized.

2. Finite difference formulation of Poisson equation

In this section we are going to introduce a 3-D electrostatic model for short channel MOSFETs taking into account the statistical nature of device physical parameters. The 3-D Poisson equation in a continuous form is expressed as

$$\nabla.\left[\varepsilon\,\nabla\psi(x,y,z)\right] = -\rho_v(x,y,z,\psi) - \rho_I(x,y,z,\psi), \tag{1}$$

where x, y, z represent the coordinates of the device along the channel length, normal to the interface and along the channel width, respectively. ε is the permittivity of the region under consideration. ψ is the electrostatic potential, ρ_I is the volume charge density, which considers the spatial and energy distribution of the interface traps charge and fixed oxide charge in the $Si\text{-}SiO_2$ interface region, and ρ_v is the volume charge density contributed by the ionized impurities, and free carriers (electrons and holes) in the semiconductor. $\rho_v(x,y,z,\psi)$ can be expressed as

$$\rho_v(x,y,z,\psi) = \begin{bmatrix} p(x,y,z,\psi) - n(x,y,z,\psi) \\ +N_D(x,y,z,\psi) \\ -N_A(x,y,z,\psi) \end{bmatrix}, \tag{2}$$

where, p, n, N_D and N_A are the free hole, free electron, ionized donor and ionized acceptor densities, respectively. In fact, for nMOSFETs, N_D takes into consideration the doping

profiles in the source and drain regions, whereas N_A takes into account the background substrate doping and the ion implantation in the channel region underneath the gate, generally used for threshold voltage adjustment.

In our model, the continuous electrostatic potential ψ is approximated by its values in a network of nodes of a non-uniform spacing 3-D rectangular grid structure with enhanced number of nodes in the regions where the structure details are of great importance (channel, source and drain regions). In the seven-point finite difference approximation, the potential value at a given node is related to the potential values at its six nearest neighbors. Fig.1 shows a node surrounded by its nearest neighbors and defines the location and potential values associated with these nodes. The perpendicular bisector planes $(Bs)_{1-6}$ of the lines joining the central node to the outside nodes define a parallelepiped V. Now, integrating Poisson's equation over V and assuming that the electric field component normal to a bisector plane is constant within this plane, we obtain the following difference equation:

$$\sum_{m=1}^{6} b_m (\psi_o - \psi_m) = -\rho_v(x_o, y_o, z_o, \psi_o) - \rho_{IS}(\psi_o), \quad (3)$$

where

$$b_m = \frac{1}{h_m V} \int_{(Bs)_m} \varepsilon ds \quad \text{and,}$$

$$\rho_{IS}(\psi_o) = \frac{1}{V} \iiint_V \rho_I(x, y, z, \psi_o) dx dy dz \quad (4)$$

In deriving Eq. (3). we have also assumed that $\rho_v(x,y,z,\psi)$ within V is constant and equal to its value at the central node, i.e. . $\rho_v(x_o,y_o,z_o,\psi_o)$.

The discrete approximation to Poisson equation is obtained by applying Eq. (3) at each node within the grid structure. The quantities associated with the nodes are represented as a 3-D array and are labeled by the node indices (i, j, k). The resulting difference equations are expressed as

$$\begin{aligned} &B_o(i,j,k)\psi(i,j,k) + B_1(i,j,k)\psi(i-1,j,k) \\ &+ B_2(i,j,k)\psi(i,j-1,k) + B_3(i,j,k)\psi(i+1,j,k) \\ &+ B_4(i,j,k)\psi(i,j+1,k) + B_5(i,j,k)\psi(i,j,k-1) \\ &+ B_6(i,j,k)\psi(i,j,k+1) = Q[\psi(i,j,k)] \\ &i = 1,\ldots,N_x \quad j = 1,\ldots,N_y \quad k = 1,\ldots,N_z, \end{aligned} \quad (5)$$

where; $\psi(i,j,k)$, $\psi(i-1,j,k)$, $\psi(i,j-1,k)$, $\psi(i+1,j,k)$, $\psi(i,j+1,k)$, $\psi(i,j,k-1)$ and, $\psi(i,j,k+1)$ represent ψ_o, ψ_1, ψ_2, ψ_3, ψ_4, ψ_5 and, ψ_6, respectively. The coefficients B_o to B_6 are given by

$$B_o = \sum_{m=1}^{6} b_m \quad \text{and} \quad B_m = -b_m, \quad (6)$$

The quantity $Q[\psi(i,j,k)]$ is simply the right hand side of Eq. (3), evaluated at the central node. The system of equations can be represented in a more compact form as a system of non-linear matrix equation. This system of equations requires the use of an iterative solution technique to get the electrostatic potential throughout the 3-D grid structure. We have applied Newton-SLOR (successive linear over relaxation) iterative technique [12] to solve this system and obtain the potential at each node in the grid structure.

3. Small-signal parameter modeling

As previously mentioned, the study of the device dynamic behavior under the influence of the statistical nature of different physical parameters as well as the 2-D nature of the channel requires an accurate small-signal device model. A non-uniform distributed TL model is an essential tool for such a type of study. Fig. 2 illustrates a 2-D version of the small-signal TL model employed in the present study. For each section of the TL model, Fig. 2-b, the capacitance C_{ox} represents the oxide capacitance, which can be expressed as

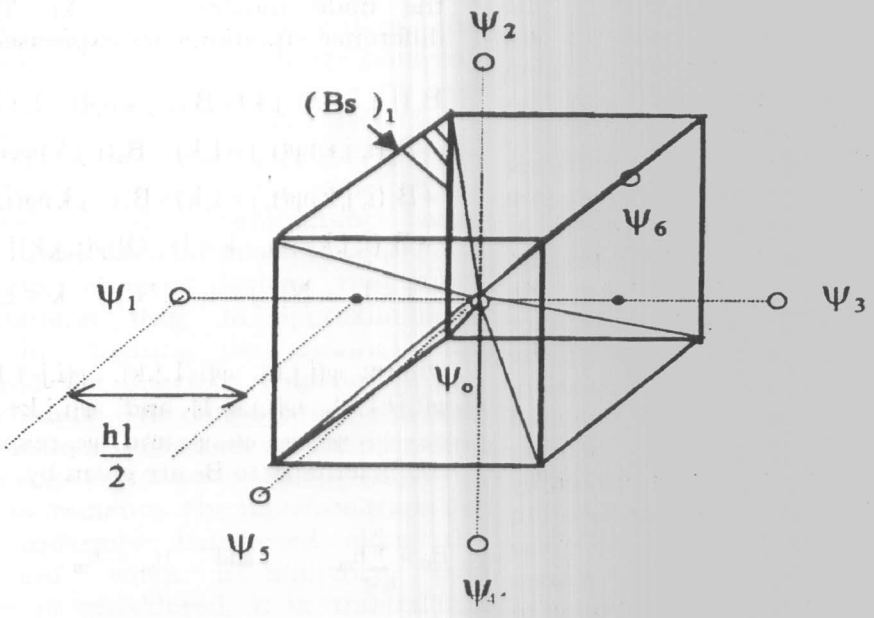


Fig. 1. An arbitrary node in the 3-D rectangular grid structure and its six nearest neighbors.

$$C_{ox}(x,z) = \frac{\varepsilon_{ox}}{d_{ox}(x,z)}\, dx\, dz\,, \qquad (7)$$

where, d_{ox} is the gate oxide thickness in the given section, ε_{ox} is the oxide permittivity, dx is the section length, and dz is the section width. The capacitance C_i represents the differential inversion layer capacitance, which is defined as

$$C_i(x,z) = \frac{dQ_i(x,z)}{d\psi_s(x,z)}\, dx\, dz\,, \qquad (8)$$

where ψ_s is the surface potential and Q_i is the inversion charge per unit area, which is given by:

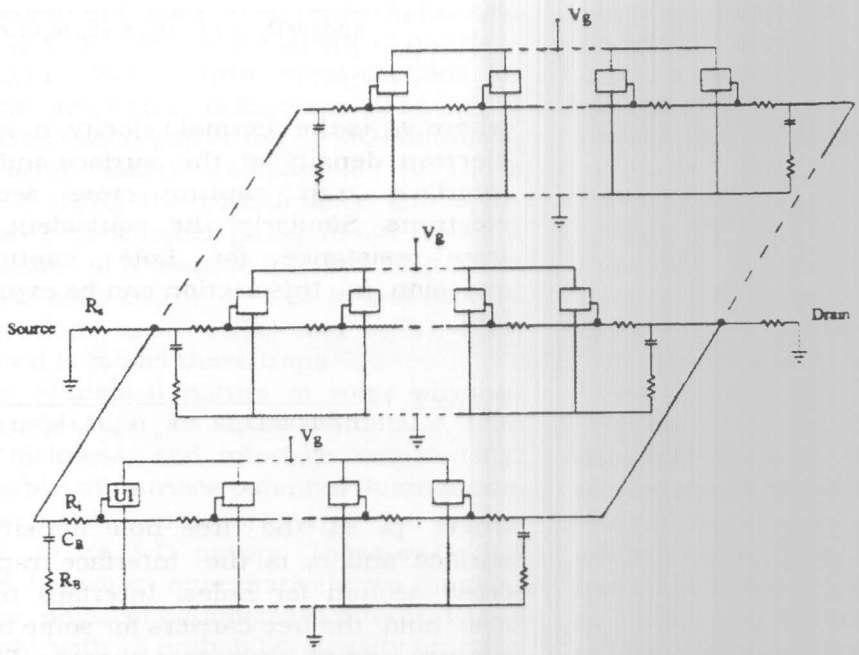
$$Q_i(x,z) = q \int_0^{'} n(x,y,z)\, dy\,. \qquad (9)$$

where q is the charge of an electron and n is the free electron density.

The capacitance C_B represents the differential depletion layer capacitance, and is given by

$$C_B(x,z) = \frac{dQ_B(x,z)}{d\psi_s(x,z)}\, dx\, dz\,, \qquad (10)$$

where Q_B is the depletion charge per unit area and is evaluated as the difference between the total semiconductor charge and inversion charge. The resistance R_i is the inversion layer resistance and is related to the channel mobile charge $Q_i(x,z)$ by [8]



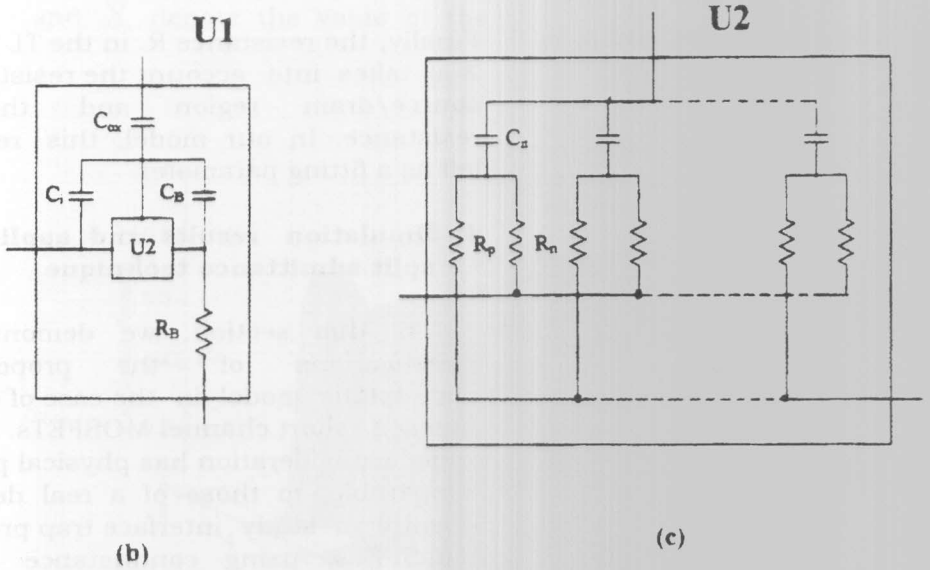


Fig. 2. (a) Non-uniform distributed TL model for short-channel MOSFETs. (b) Details of U1. (c) Details of U2.

$$R_i(x,z)=\frac{dx}{|Q_i(x,z)|\,\mu_{eff}\,dz}, \qquad (11)$$

where μ_{eff} is the effective channel mobility and is expressed as [13]

$$\mu_{eff}=\frac{\mu_o}{1+\frac{E_{eff}}{E_c}} \quad \text{with,} \quad \mu_o=\frac{\mu_{oo}}{1+\alpha\left(Q_f+qD_{it}\right)}$$

$$\text{and} \quad E_{eff}=\frac{1}{\varepsilon_{si}}\left(Q_B+\frac{Q_i}{2}\right).$$

where μ_o is the low field mobility, E_{eff} is the effective transversal electric field across the channel, E_c is the critical electric field, Q_f is the fixed oxide charge density, and D_{it} is the interface trap density. The parameters μ_{oo} and α are functions of doping concentration. The resistance R_B is the bulk resistance, and is expressed as

$$R_B(x,z)=\frac{d}{q\,\mu_p\,N_A\,dx\,dz}, \qquad (12)$$

where d is the substrate thickness, and μ_p is the hole mobility in the bulk.

The small-signal circuit elements R_n, R_p and C_{it} (Fig. 2-c) model the dynamic behavior of interface traps at the Si-SiO_2 interface. These traps have energy levels located within the silicon band gap. The traps can interact with the silicon conduction and valance bands by capturing or emitting free carriers. The probability $f_o(E_n)$ that an interface trap level is occupied by an electron is determined by the Fermi function:

$$f_o(E_n)=\frac{1}{1+\exp(\beta(E_n-E_F))}, \qquad (13)$$

where E_n is the trap energy level and E_F is the Fermi energy level. For each trap level the equivalent interface trap resistance for electron capture and emission in a section of area (dx dz) can be expressed as [14]

$$R_n(x,z,E_n)=\frac{1}{q\beta dx\,dz\,D_{it}(x,z,E_n)\,v_{th}\,\sigma_n(E_n)\,n_s(x,z)(1-f_o(E_n))} \qquad (14)$$

where v_{th} is the thermal velocity. n_s is the free electron density at the surface and σ_n is the interface trap capture cross section for electrons. Similarly, the equivalent interface trap resistance for hole captures and emission in this section can be expressed as [14]

$$R_p(x,z,E_n)=\frac{1}{q\beta\,dx\,dz\,D_{it}(x,z,E_n)\,v_{th}\,\sigma_p(E_n)\,p_s(x,z)\,f_o(E_n)} \qquad (15)$$

where p_s is the free hole density at the surface and σ_p is the interface trap capture cross section for holes. Interface traps can also hold the free carriers for some time after capture and so, they store charges. Therefore, there will be a capacitance C_{it} proportional to the interface trap density and is given by [14]

$$C_{it}(x,z,E_n)=dz\,dx\,q\beta\,D_{it}(E_n)f_o(1-f_o). \qquad (16)$$

Finally, the resistance R_s in the TL model (Fig. 2-a) takes into account the resistance of the source/drain region and the contact resistance. In our model, this resistance is left as a fitting parameter.

4. Simulation results and application to split admittance technique

In this section, we demonstrate the investigations of the proposed 3-D electrostatic model in the case of electrically stressed short channel MOSFETs. The device under consideration has physical parameters comparable to those of a real device used recently to study interface trap properties in nMOSFETs, using conductance and split-admittance techniques [9,11]. The physical and simulation parameters used in our model are shown in Table.1

The doping profiles in the source, drain and channel regions have been modeled using Gaussian distribution functions. Source and drain lateral diffusions

underneath the gate oxide have been also taken into account. The density of interface traps and their capture cross-sections for electrons and holes, as functions of energy in the silicon band-gap at the Si-SiO_2 interface, have been taken comparable to those extracted using the conductance and split-admittance techniques [9,11]. In our model, a distribution of N discrete interface trap levels with a density $D_{it}(E_n)$, n =1,2,..N, and capture cross-section areas $\sigma_n(E_n)$ and $\sigma_p(E_p)$, have been used to model these traps.

The statistical nature of some physical parameters such as substrate doping, gate oxide thickness, and interface trap density, responsible of surface potential fluctuations, can be easily incorporated in the model; thanks to its 3-D nature. To express this random behavior quantitatively, we consider that the physical parameter of interest varies randomly with a probability density function of the form:

$$P(X) = \frac{1}{\sqrt{2\pi}\,\sigma_X} \exp\left(-\frac{(X-\overline{X})^2}{2\sigma_X^2}\right), \qquad (17)$$

where X and $\overline{X}$ denote the value of the physical parameter under consideration and its mean value, respectively, and σ_X is the standard deviation of the distribution.

Figure 3 shows the electrostatic potential distribution at different planes parallel to the xy-plane throughout the 3-D grid structure, for a given value of gate voltage in the weak inversion regime. The influence of the statistical nature of physical parameters is greatly pronounced in this figure in the form of potential fluctuations within the device. For the sake of clarity and interpretation, the surface potential ψ_s along the channel (coordinate x) at different positions in the xz-plane is illustrated in Fig. 4. It is noted that ψ_s represents a plateau with enhanced fluctuations in the mid-region of the channel and increases progressively when approaching the source and drain ends. This is conventionally attributed to the 2-D nature of the channel in short channel devices. the channel and increases progressively when approaching the source and drain ends. This is conventionally attributed to the 2-D nature of the channel in short channel devices.

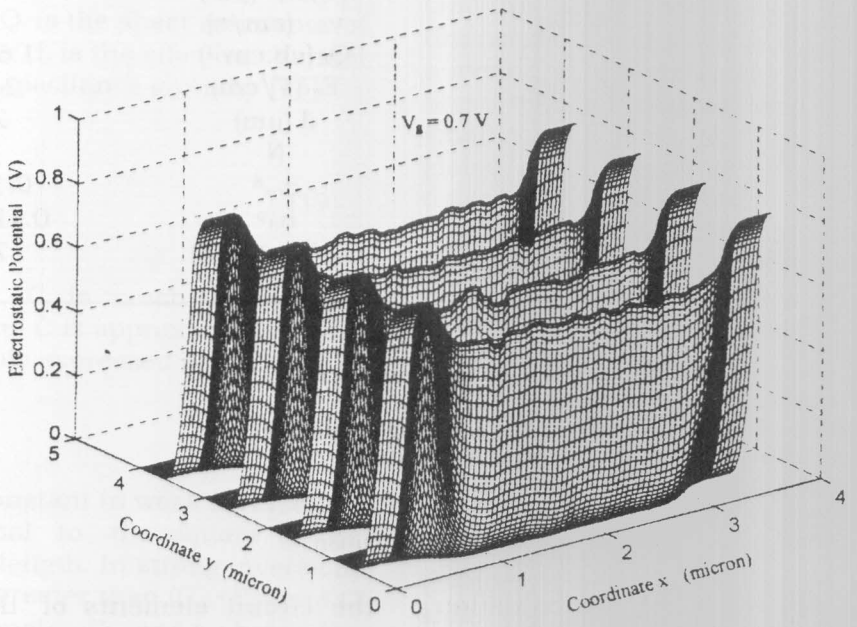


Fig. 3. Electrostatic potential distribution at different planes parallel to the xy-plane, including the effect of statistical distributions of different physical parameters.

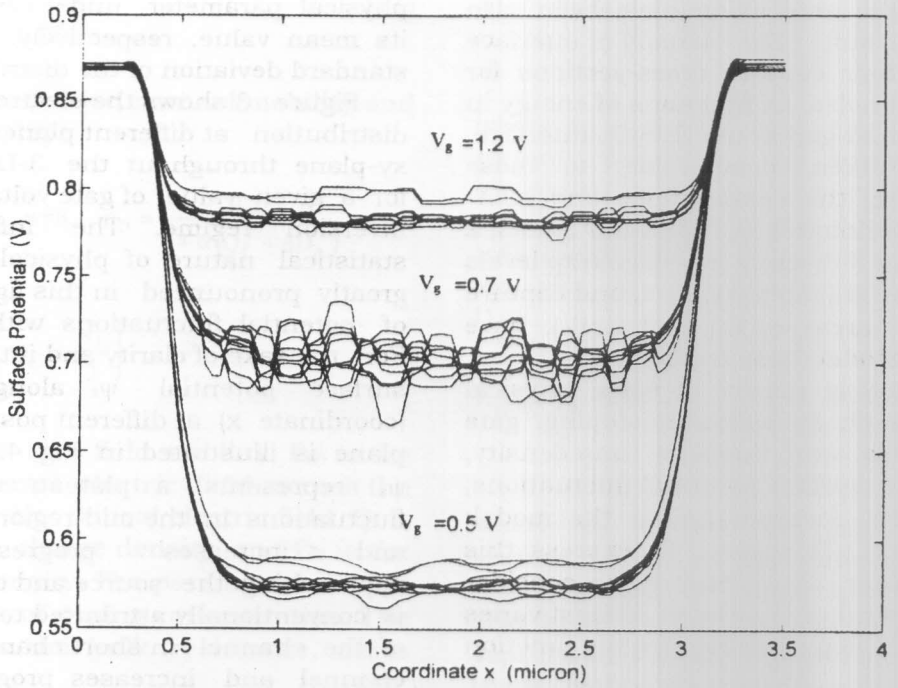


Fig. 4. Surface potential distribution at different positions in the xz-plane, including the effect of statistical distributions of different physical parameters, with the gate voltage as parameter.

Table 1. Device physical and simulation parameters.

Parameter	Value	Parameter	Value
d_{ox} (A°)	250	$(d_j)_{S,D}$[7] (μm)	0.25
W[1] (μm)	6000	v_{th} (cm/s)	10^7
L_{eff}[2] (μm)	3	Q_f (cb.cm^{-2})	1.6×10^{-9}
N_A (cm^{-3})	2×10^{16}	E_c (V/cm)	2×10^5
N_D (cm^{-3})	10^{19}	d (μm)	200
N_{AP}[3] (cm^{-3})	8×10^{17}	N	24
y_p[4] (μm)	0.02	σ_{ox}[8]	$0.15d_{ox}$
σ_I[5]	0.06	σ_{it}[9]	$0.1D_{it}(x,z)$
α	0.2	μ_{oo} (cm^2/V.S)	700
σ_{NA}[6]	$0.13\ N_A$		

1. channel width.
2. channel length.
3. maximum acceptor concentration in the ion-implanted layer.
4. projected range in the ion implanted-layer.
5. standard deviation of the ion-implanted layer doping distribution.
6. standard deviation of the substrate doping distribution.
7. junction depth of drain / source.
8. standard deviation of the oxide thickness.
9. standard deviation of the interface trap density distribution.

As discussed in section 3, the determination of $\psi(x,y,z)$ is the key point in the evaluation of all other unknowns; namely, n(x, y, z), p(x, y, z), inversion layer charge Q_I, depletion layer charge Q_B and interface trap charge Q_{it}. Thus, the circuit elements of the TL model can be evaluated in a straightforward manner. In the split-admittance technique, a small ac signal is superimposed on the dc gate bias while the source, drain and substrate are tied together

and grounded. The gate-channel and gate-substrate conductance G_{gc} and G_{gb} and capacitance C_{gc} and C_{gb} as a function of frequency are obtained from the real and imaginary parts of the small-signal currents measured in the source/drain and substrate circuits [11]. In order to permit such a type of study in our case, the TL model of Fig. 2-a is implemented in a circuit simulator (SPICE), resulting in the required split-conductance and -capacitance. As mentioned previously, the conductance-based techniques assume that the channel time constant in relatively short channel devices operating in the weak and strong inversion is negligibly small compared with 1/f up to frequencies of tens of MHz. This permit to neglect the channel resistance and consequently the TL model can be simplified to its lumped-element small-signal version. In fact, a detailed analysis of a TL model using uniformly distributed elements and neglecting interface traps, has shown that the channel time constant τ_{gc} is given by [15]

$$\tau_{gc} = \frac{C r_i L^2}{4} , \qquad (18)$$

where $r_i = 1/\mu_{eff}\ Q_i$ is the sheet resistance of the inversion layer, L is the effective channel length and C is a capacitance given by [15]

$$C = \frac{C_i (C_{ox} + C_B)}{C_i + C_B + C_{ox}} . \qquad (19)$$

In weak inversion, C_i is much smaller than $(C_{ox}+C_B)$ and hence C is approximately equal to C_i, which is simply expressed as [15]

$$C_i = \beta Q_i . \qquad (20)$$

As a result, τ_{gc} is constant in weak inversion and is proportional to the square of the effective channel length. In strong inversion, C_i becomes much greater than $(C_{ox}+C_B)$ and C is approximately equal to C_{ox} and τ_{gc} becomes:

$$\tau_{gc} \cong \frac{C_{ox} L^2}{4\mu_{eff} Q_i} . \qquad (21)$$

This indicates that τ_{gc} decreases with increasing V_g due to the rapid increase of Q_i and tends to saturate at relatively high V_g values due to μ_{eff} reduction [10]. To test this point in our study, in which the 2-D nature of the channel is taken into account, a simulation has been carried out without the presence of interface traps. The simulation results obtained for G_{gc}/ω (ω being the angular frequency) as a function of frequency are illustrated in Fig. 5.

In weak inversion ($V_g < 0.7V$), it is noted that at a given value of V_g, G_{gc}/ω exhibits a peak shifting towards higher frequencies when increasing V_g. This result indicates that the channel time constant τ_{gc} decreases progressively with increasing V_g in weak inversion, in contradiction with that was previously predicted from the simple one-dimensional theory. A simple interpretation of this behavior is attributed to the 2-D nature of the channel. In weak inversion, the mid-region of the channel is weakly inverted resulting in high r_i values and small C_i values. On the other hand, near the source and drainends, the channel is strongly inverted as a result of the presence of the source and drain diffused regions, and thus resulting in small values of r_i, and high values of C_i. A global effect overall the channel, is a slight decrease in the effective channel resistance $(R_i)_{eff}$ and a considerable increase in the effective inversion layer capacitance $(C_i)_{eff}$, resulting in a greater channel time constant compared with that predicted from the one-dimensional theory. As V_g increases, the value of r_i in the mid-region of the channel decreases and C_i increases, but is still much smaller than its value in the source and drain end regions. This will result in a decrease in $(R_i)_{eff}$, while $(C_i)_{eff}$ remains essentially unchanged. The result is a decrease in the channel time constant, and consequently a shift of the peak of G_{gc}/ω towards higher frequencies. In strong inversion ($V_g > 0.7V$), the channel is strongly inverted everywhere and the values of r_i and C_i in the mid-region

approach their values in the source and drain end regions and the simple one-dimensional theory would apply. The peak of G_{gc}/ω shifts slightly towards higher frequencies due to the converse behavior of Q_i (V_g) and μ_{eff} (V_g) as previously explained.

The above results of the frequency response of G_{gc}/ω in weak inversion are surprisingly important, as the peak of the response varies in a frequency range from few tens of Hz up to few MHz. Keeping in mind that this range is typically the frequency range of the interface trap conductance response [11], it is concluded that in the presence of interface traps, G_{gc}/ω is affected not only by the interface trap response but also by the channel response. To highlight this point in our study, simulations have been carried out in the presence of statistical distribution of interface traps. The obtained results of G_{gc}/ω as a function of frequency are shown in Fig. 6. It is seen that the G_{gc}/ω exhibits a relatively wide peak, which is attributed to the merged responses of both the interface traps and the channel itself. From the above discussion. it can be concluded that the interface trap properties extracted from the conductance and conductance-based technique in MOSFETs, are affected by the channel time constant. In fact, the extracted interface trap density may be overestimated using such techniques. To clarify this point in our study, the simulation results of G_{gc}/ω are plotted as a function of V_g with the frequency as a parameter as shown in Fig. 7 and compared with the measured characteristic [11]. Keeping in mind that the interface trap properties used in the simulation are those obtained from the

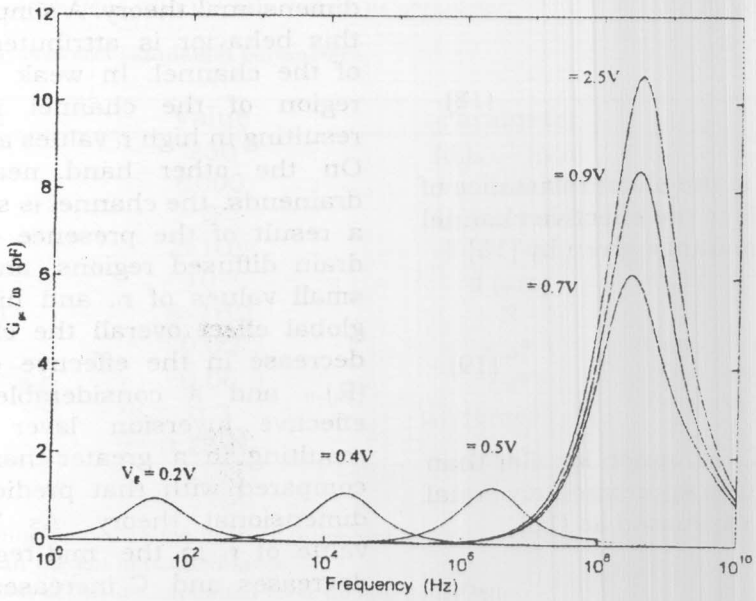


Fig. 5. Simulation results of G_{gc}/ω as a function of frequency at different gate voltages in the absence of interface traps.

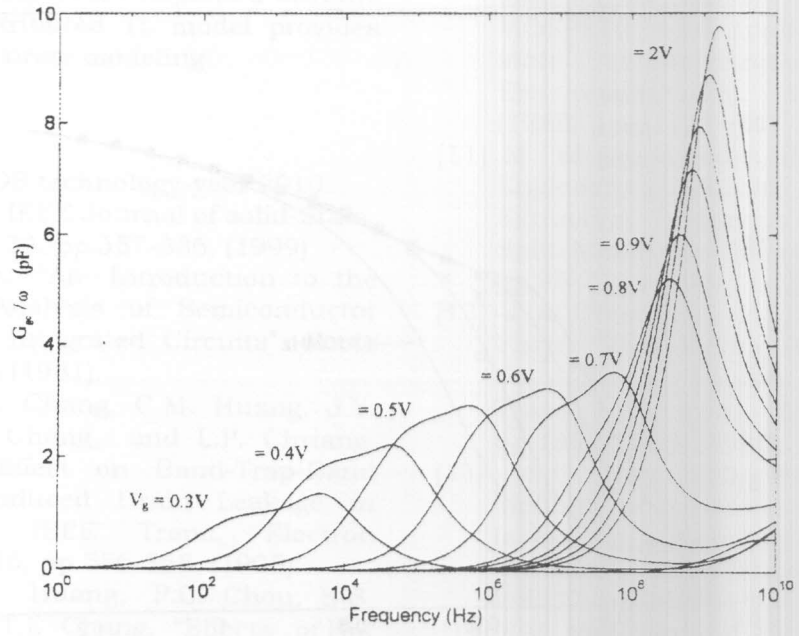


Fig. 6. Simulation results of G_{gc}/ω as a function of frequency at different gate voltages in the presence of statistical distribution of interface traps and other physical parameters.

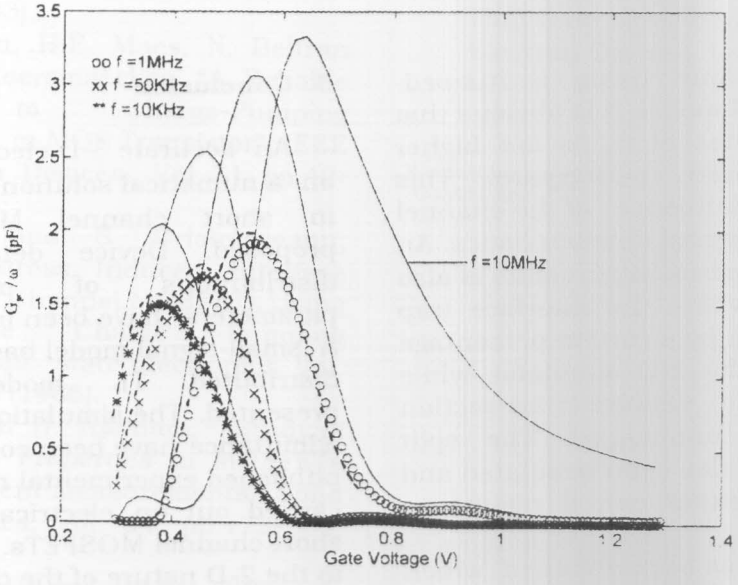


Fig. 7: Comparison between the simulation results (solid curves) of the G_{gc}/ω as a function of gate voltage and experimental data (symbols) at different operating frequencies. The dashed curves represent the simulation results fitting the experimental data.

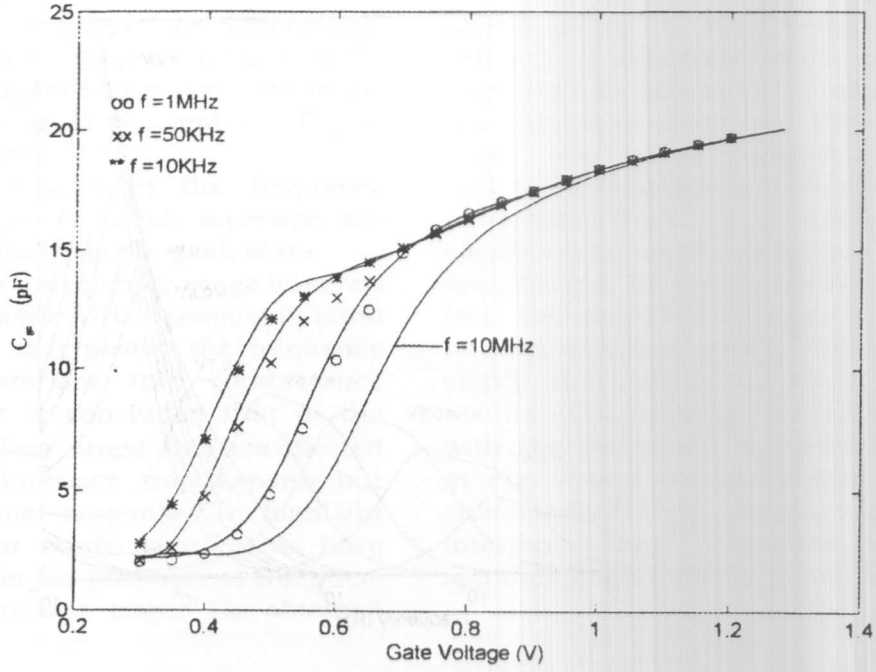


Fig. 8. Comparison between the simulation results (solid curves) of the C_{gc} as a function of gate voltage and experimental data (symbols) at different operating frequencies.

conductance technique using a lumped-element small-signal model, it is obvious that the simulation values of G_{gc}/ω are higher than their measured counterparts. This clearly reflects the influence of the channel response on the measured characteristics. An attempt to fit the experimental results is also shown in Fig. 7, where the interface trap density is decreased by a certain percentage and introduced in the 3-D simulator while keeping the extracted capture cross-section areas σ_n and σ_p unchanged. The split capacitance C_{gc} has also been simulated and compared with the experimental results as shown in Fig. 8.

Satisfactory fitting has been obtained, which reflects the accuracy of the proposed model.

Split-conductance G_{gb} and capacitance C_{gb} characteristics, measured in the substrate circuit, have also been successfully simulated and compared with their experimental counterparts.

5. Conclusion

An accurate 3-D electrostatic model based on a numerical solution of Poisson's equation in short channel MOSFETs has been proposed. Device details and statistical distributions of important physical parameters have been included in the model. A small-signal model based on a non-uniform distributed TL model has also been presented. The simulation results of the split-admittance have been compared with recently published experimental results carried out on electrically stressed relatively short channel MOSFETs. It is noted that due to the 2-D nature of the channel, the split-Conductance in such short channel devices is affected not only by the induced interface traps but also by the channel response itself. As a result, the interface trap density extracted using such techniques may be overestimated, and accurate static and small-signal models have to be used. The proposed

3-D electrostatic model accompanied with the non-uniform distributed TL model provides such a type of accurate modeling.

References

[1] H. Iwai, "CMOS technology-year 2010 and beyond," IEEE Journal of solid-State Circuits, Vol. 34, pp.357-336, (1999).

[2] J.J.H. Miller, "An Introduction to the Numerical Analysis of Semiconductor Devices and Integrated Circuits", Boole Press, Dublin (1981).

[3] T. Wang, T.E. Chang, C.M. Huang, J.Y. Tang, K.M. Chang, and L.P. Chriang, "Structural Effect on Band-Trap-Band Tunneling Induced Drain Leakage in nMOSFETs", IEEE Trans. Electron Devices, Vol.16, pp.556-568, (1995).

[4] T. Wang, C. Huang, P.C. Chou, S-S. Chung, and T.E Chang, "Effects of Hot Carrier Induced Interface State Generation in Submicron LDD MOSFETs", IEEE Trans. Electron Devices, Vol. 41, pp.1618-1622, (1994).

[5] S.M. Sze, "VLSI Technology", McGraw-Hill Singapore, (1983).

[6] G. Groeseneken, H.E. Maes, N. Beltran and R.F. Dekeersmaecker, "A Reliable Approach to Charge-Pumping Measurements in MOS Transistor", IEEE Trans. Electron Devices, Vol. 31, pp.42-48, (1984).

[7] H. Haddara and S. Cristoloveanu, "Profiling of Stress Induced Interface States in Short Channel MOSFETs Using a Composite Charge Pumping Technique", Solid state Electronics, Vol. 29, pp.767-772, (1986).

[8] M. El-Sayed and H. Haddara, "Study of Interface Trap Properties in MOSFETs using split-current measurements", Solid state Electronics, Vol. 34, pp.173-180, (1991).

[9] H. Haddara and M. El-Sayed, "Conductance technique in MOSFETs: Study of Interface Trap Properties in the depletion and weak inversion regimes", Solid state Electronics, Vol. 31, pp.1289-1298, (1988).

[10] H. Haddara and G. Ghibaudo, "Analytical Modeling of Transfer Admittance in Small MOSFETs and Application to interface state characterization", Solid state Electronics, Vol. 31, pp.1077-1082, (1988).

[11] M. El-Sayed and H. Haddara, Alexandria Engineering Journal, "A New Parameter Extraction Technique in MOSFETs Using Split-Admittance Measurements", Vol.35, pp.95-110 (1996).

[12] J. A. Greenfield, and R. W. Dutton, "Non-Planer VLSI Device Analysis Using the Solution of Poisson Equation", IEEE Trans. Electron Devices, Vol. 27, pp.1522-1530, (1980).

[13] S.C. Sun, J.D. Plummer, "Electron Mobility in Inversion and Accumulation layers on Thermally Oxidized Silicon Surfaces", IEEE Trans. Electron Devices, Vol. 27, pp.1497-1508, (1980).

[14] E.H. Nicollian and J.R. Brews, "MOS Physics and Technology", New York, John Willy & Sons, (1981).

[15] P.D. Chow and K. Wang, "A New AC Technique for Accurate Determination of Channel Charge and Mobility in Very Thin Gate MOSFETs" , IEEE Trans. Electron Devices. Vol. 33, pp.1299-1304, (1986).

Received January 24, 2000
Accepted April 15, 2000