

PROBABILISTIC ANALYSIS OF FAULT DETECTION IN COMPLEX LOGIC CIRCUITS

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ABSTRACT

Generation of test patterns for combinational logic circuits is a search through the set of all input values to find the one that causes the output of a faulty circuit to differ from that of a good one. This paper conducts the analysis aiming at detecting faults for most commonly used logic circuits of complex structure. It relates the obtained results to redundant circuits, to circuits with multiple fan-in, to mesh structured circuits and to circuits with feedback connection. Probability transfer function, fixed point bias probability, path sensitization probability and optimum number of tests are determined for each circuit structure. The condition for the use of random testing are also specified. The conducted analysis proved to be valid for the particular structures previously introduced in the literature.

Key words

Complex logic circuits, fault detection, feedback, mesh structure, multiple fan-in, path sensitization, probabilistic analysis, redundant logic circuits.

1. INTRODUCTION

Fault detection in logic circuits is testing the circuit to determine whether or not it functions correctly. The process of fault detection terminates either when a sufficiently large number of inputs is applied so that it can be certified that the circuit is fault free, or when an erroneous output is detected. Fault correction is the process of finding the reason which caused an erroneous output, and eliminating this reason. The evolution of logic circuits from discrete components to VLSI technology had a dramatic effect on both.

The problem of fault detection became more complicated. While it was perfectly feasible to test an SSI chip by trying all input combinations exhaustively, this approach is not suitable for a VLSI chip with, say, 40 inputs and 10^7 gates on the wafer, since in such case an exhaustive test would require the generation of 2^{40} input combinations. This is too time consuming to be practical. Fault correction, on the other hand, became simpler. Circuits composed of LSI and VLSI chips tend to exhibit modular structure, and they are composed of a much smaller number of replaceable components [1]. This implies that it is sufficient to trace a fault to a VLSI chip, which makes fault

correction manageable. Fault correction is not included in this paper, but it is treated in [2] which describes a general algorithm for correcting an error in a logic circuit.

Fault detection was treated in [3], [4], [9] and [10]. A relation between the number of test generations, and the degree of confidence in test results (the probability that the circuit is error free) is proposed. It was found that to reduce testing time, it is required to achieve the desired confidence (probability) with the minimum number of test generations. Input patterns are generated at random.

In [3] it was stated that if the circuit is to be certified error free with probability P , one must generate M test patterns, where:

$$M = \frac{\log (1-p)}{\log (1-p_s)} \quad (1)$$

and P_s is the probability of finding the error by applying one input pattern only. The equation is general and may be applied to any circuit.

Since P is usually given, fault detection focusses on finding the value of P_s which minimizes M (the duration of the test). Once P_s is obtained, it is substituted in Eq. 1 and M is calculated for the given P . The random test is then conducted M times. If no error is detected the circuit is certified error free with probability P , else it is rejected as faulty. An expression for P_s is obtained for a non-redundant NAND tree structure. It is shown that :

$$P_s = (P_0^1)^{n-1} (P_1^1)^{n-1} \dots (P_{L-1}^1)^{n-1} \quad (2)$$

where:

P_k^1 is the probability of occurrence of logic 1 at input of level k .

n is the NAND gate fan-in.

L is the number of levels in the tree.

P_k^1 and P_{k-1}^1 are related by the following equation:

$$P_k^1 = 1 - (P_{k-1}^1)^n \quad (3)$$

From Eq. 2 it turns out that P_s is a function of the external input bias probability P_0^1 which is the probability of occurrence of logic 1 at level 0. In fact substituting from Eq.3 into Eq.2 recursively, we may express P_s exclusively in terms of P_0^1 . This suggests that the input bias probability P_0^1 has a direct effect on the required number of test generations, since it determines the value of P_s which affects the value of M as indicated in Eq.1. Thus it is required to find the input bias probability which minimizes M . This issue is treated in [4] for non-redundant AND-OR tree structure. It is proved that this circuit structure has a probability transfer function given by :

$$P_Y = [1 - (1 - P_u)^m]^n \text{ or}$$

$$P_Y = 1 - (1 - P_u^n)^m \quad (4)$$

where m and n denote the fan-in of OR and AND gates respectively. P_Y and P_u are the output and input bias probabilities respectively. The circuit has a fixed point when $P_u = P_Y$. It is stated in [4] that to minimize the number of test generations M , the input bias probability has to be equal to the fixed point bias probability. This result is used here to find the

minimum number of test generations M which gives the required measure of confidence P . The question of how to run the tests is treated in [5],[6],[7],[11],[13].

This paper extends fault detection results of [3],[4] to more general but non-exhaustive circuit structures. The restricting assumptions of pure tree structure, and of nonredundant circuits are relaxed. Also, circuits of mesh structure with multiple fan-in are analysed. The effect of feedback on the analysis is studied.

The following simplified procedure is followed for circuit analysis :

Procedure (1):

- 1- Find the fixed point probability (if one exists).
- 2- Set the input probability equal to the fixed point probability. This, according to [4], minimizes the test length.
- 3- Calculate P_s from the input probability obtained in step (2).
- 4- Substitute P_s in Eq.1 to find M .
- 5- Apply M random patterns to the circuit.
- 6- If no error is detected the circuit is certified to be error free with probability P .
- 7- If an error is detected the circuit is rejected as faulty. If the circuit is faulty, a fault correction algorithm may be invoked (not treated in this paper).

Relaxing the non-redundancy assumption, its consequences and a theoretical approach to deal with it are described in section 2, which develops the necessary tools for the analysis conducted in Section 3. Section 3 conducts the necessary analysis for different circuit topologies. Section 4 compares between random testing and the exhaustive testing. Section 5 summarizes the conclusions about the effect of circuit topology, feedback, redundancy, and multiple fan-in on the optimal selection of input bias probability which minimizes the number of test generations required.

Issues of controllability and observability of the proposed topologies are not explicitly studied in this work, but for specific details [12] presents an evaluation of the computational complexity of controllability and observability in combinational circuits.

2. PROBABILISTIC ANALYSIS OF LOGIC CIRCUITS :

This section develops the theoretical basis necessary for analyzing the proposed circuits of complex structure. The section is organized as follows : Subsection 2.1 describes the problem resulting from relaxing the non-redundancy assumption. Subsection 2.2 builds the tools to analyse redundant circuits. Subsection 2.3 discusses the complications resulting from introducing feedback and derives a set of tools to deal with these complications. Subsection 2.4 generalizes the developed tools so that they may be applied to multiple fan-in circuits.

2.1 Redundant Circuits

The approach taken in [3] and [4] to find probability transfer functions of logic circuits assumes that all gate inputs are independent. This limiting assumption follows from the nonredundancy assumption. The probability of any joint event $\{A\}$ and $\{B\}$ is the product of individual probabilities of events $\{A\}$ and $\{B\}$. That is:

$$P \{A, B\} = P \{A\} P \{B\} \quad (5)$$

where $P \{A, B\}$ denotes the probability of the joint event $\{A\}$ and $\{B\}$, with events A and B denoting the occurrence of high level (logic level 1) at corresponding lines in the circuit. Eq.5 may not hold in the general case of redundant circuits.

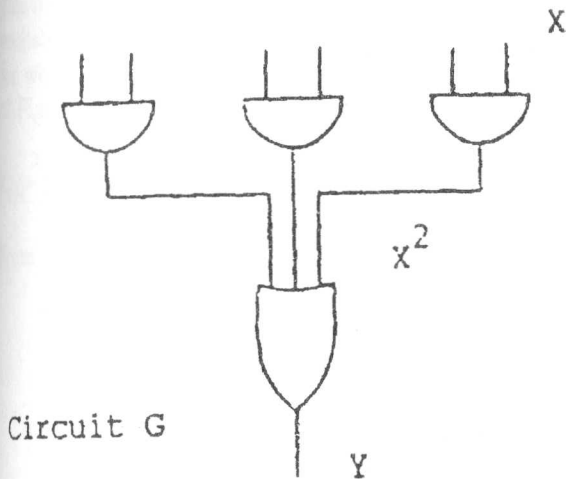


Figure 1. Redundant circuit: case 1.

Consider, for instance, circuit G shown in Figure (1). According to [4] its probability transfer function is:

$$y = 1 - (1 - x^2)^3$$

where \bar{x} , y are the input and output bias probabilities respectively. For a redundant circuit $y=x$.

Now, for the circuit shown in Figure (2), what is the probability transfer function between y and z (z is the input bias probability) ?

Since we know that $y = 1 - (1-x^2)^3$ and noting that $x=z$, we get:

$y = 1 - (1 - z^2)^3$. This, unfortunately, is not correct. The correct solution is $y = z$.

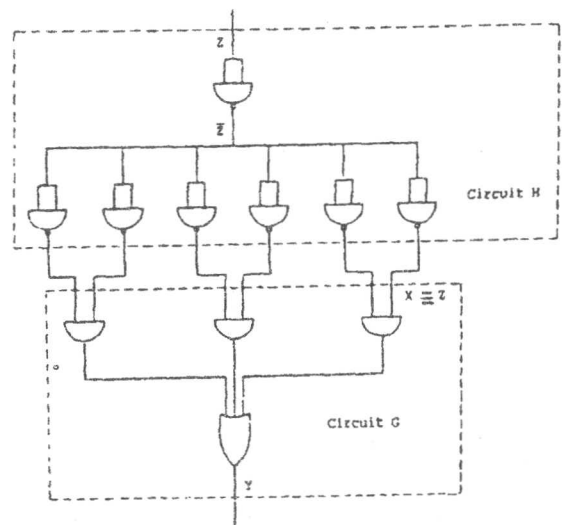


Figure 2. Redundant circuit: case 2.

Since, when the input to circuit H is 1, all its outputs, which are inputs to circuit G, are 1's. Thus each AND gate in G has two 1's on its inputs yielding a 1 at its output. The three AND gates have a 1 at the output, the OR gate has a 1 at the output too. Similarly when the input to circuit H is 0, all its outputs, which are inputs to circuit G, are 0's. Thus each AND gate in G has two 0's on its inputs yielding a 0 at its output. Since all three AND gates have a 0 at their outputs, the OR gate has a 0 at its output too. Thus, when the input to the combined circuit is 1, its output is 1, and when the input to the combined circuit is 0, its output is 0. Thus the output is always the same as the input, i.e. the overall probability transfer function is $y = z$, not $y = 1 - (1 - z^2)^3$.

This conclusion is justified by noting that the outputs

of circuit H, (which are inputs to circuit G) are not independent. Thus the expression : $y = 1 - (1-x^2)^3$ for the probability transfer function of circuit G is no longer valid, since it assumes that all inputs are independent (see [4]). In other words, Eq.5 is not satisfied. An additional approach should then be proposed.

2.2 Tools for Analyzing Redundant Circuits

The goal of this subsection is to develop an alternative to Eq. 5. It is required to calculate $P \{A, B\}$ in the case when events A and B are correlated. A and B are correlated if lines A and B have a common origin, i.e. they may be traced back to a common signal (see Figure (3)).

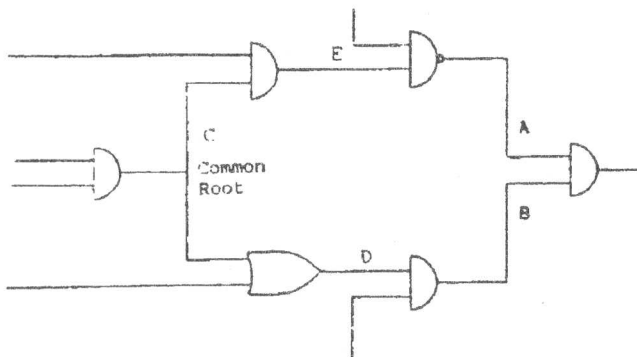


Figure 3. Analysis of redundant circuits

It is to be noted that since A and B are binary events, $P \{A, B\}$ is also the cross-correlation between A and B, denoted by $R(A,B)$:

$$R(A,B) = E\{AB\} = 1x1xP\{A,B\} + 1x0xP\{A,\bar{B}\} + 0x1xP\{\bar{A},B\} + 0x0xP\{\bar{A},\bar{B}\} = P\{A,B\}$$

Thus, from now on, $P \{A, B\}$ will be referred to by correlation. P and R will be used interchangeably. Note that in the special case where A and B are the same event (which means that A and B are the same line or two branches of the same line) we have :

$$R(A, B) = P \{A, B\} = P \{A, A\} = P \{A\} \quad (6)$$

The steps to find the correlation between A and B, $R(A,B)$ are given in the following procedure:

Procedure (2):

- 1- Find the common root signal C.
- 2- From Eq.13 (to be derived later), find correlation of this signal with its output $R(\bar{C},C)=P(C)$.
- 3- Use a Correlation Propagation Law recursively (the law is to be derived later) to find correlation between the next pair of signals descending from the common root until signals A and B are reached and $R(A,B)$ is calculated for them (see Figure (4)).

- | | | |
|----|------|----------|
| 1. | Find | R_{CD} |
| 2. | Find | R_{ED} |
| 3. | Find | R_{EB} |
| 4. | Find | R_{AB} |

Figure 4. Steps of the analysis.

In what follows only two-input gates are studied, a gate has more than two inputs, it can be decomposed into several gates each of which has exactly two inputs (as shown in Figure (5)). Subsection 2.4 extends this analysis to the case of multiple fan-in.

Theorem (1): (The Correlation Propagation Law).

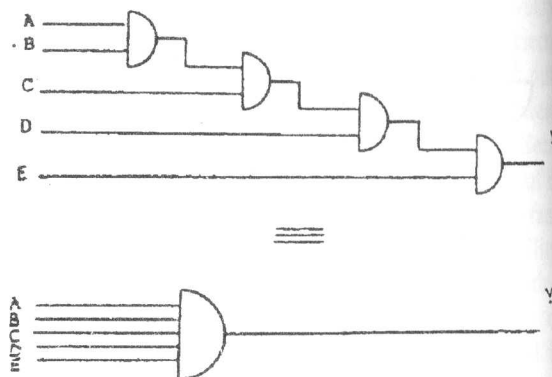


Figure 5. Representation of a multiple fan-in gate.

If X_1, X_2 are the two inputs, and Y is the output of a gate, which implements the function given by

truth table in Figure (6-a), where d_0, \dots, d_3 have the values 0 or 1, then for any external Boolean event A we have:

$$R_{YA} = P_A d_0 + R_{X1A}(d_2-d_0) + R_{X2A}(d_1-d_0) + R_{X1X2A}(d_3-d_0-d_1-d_2) \quad (7)$$

where:

R_{YA} is the correlation between the output Y and event A.
 d_0, \dots, d_3 define the truth table of the gate (see Figure (6-a)).

R_{X1A} , R_{X2A} and R_{X1X2A} are the cross-correlations between the respective input signals and event A.

X_1	X_2	Y
0	0	d_0
0	1	d_1
1	0	d_2
1	1	d_3

(a)

X_1	X_2	A	Y
0	0	0	d_0
0	0	1	d_0
0	1	0	d_1
0	1	1	d_1
1	0	0	d_2
1	0	1	d_2
1	1	0	d_3
1	1	1	d_3

(b)

Figure 6. Correlation propagation law.

Proof:

Since we are dealing with binary logic, then $R_{YA} = P_{YA}$, but P_{YA} is the probability that both the gate output Y, and the external signal A are high. This probability is the sum of probabilities of all minterms for which $Y=1$ and $A=1$ in the augmented truth table of Figure (6-b), i.e.:

$$P_{YA} = P_{\bar{X}_1 \bar{X}_2 A} d_0 + P_{\bar{X}_1 X_2 A} d_1 + P_{X_1 \bar{X}_2 A} d_2 + P_{X_1 X_2 A} d_3 \quad (8)$$

From Set Theory we have:

$$P_{\bar{X}_1 \bar{X}_2 A} = (P_A - P_{X_1 A} - P_{X_2 A} + P_{X_1 X_2 A})$$

$$P_{\bar{X}_1 X_2 A} = (P_{X_2 A} - P_{X_1 X_2 A})$$

$$P_{X_1 \bar{X}_2 A} = (P_{X_1 A} - P_{X_1 X_2 A}) \quad (9)$$

Substituting from Eq.9 into Eq.8, and rearranging:

$$R_{YA} = P_A d_0 + P_{X_1 A} (d_2-d_0) + P_{X_2 A} (d_1-d_0) + P_{X_1 X_2 A} (d_3+d_0-d_1-d_2) \quad (10)$$

and since joint probability and correlation are the same for binary events, we may rewrite the above equation as:

$$R_{YA} = P_A d_0 + R_{X_1 A} (d_2-d_0) + R_{X_2 A} (d_1-d_0) + R_{X_1 X_2 A} (d_3+d_0-d_1-d_2)$$

which is the same as Eq.7. The theorem is thus proved.

An interesting case results if event A is the global event S. By replacing each A by S in Eq.7 the theorem is rewritten as :

$$R_{YS} = P_S d_0 + R_{X_1 S} (d_2-d_0) + R_{X_2 S} (d_1-d_0) + R_{X_1 X_2 S} (d_3+d_0-d_1-d_2) \quad (11)$$

It will be proved that Eq.11 gives the output bias probability of the gate. Replacing correlation for probabilities (valid for Boolean signals only), and using the fact that $P_s=1$, Eq.11 reduces to :

$$P_Y = d_0 + P_{X_1} (d_2-d_0) + P_{X_2} (d_1-d_0) + P_{X_1 X_2} (d_3+d_0-d_1-d_2) \quad (12)$$

$$= (1-P_{X_1}-P_{X_2}+P_{X_1 X_2})d_0 + (P_{X_2}-P_{X_1 X_2})d_1 + (P_{X_1}-P_{X_1 X_2})d_2 + P_{X_1 X_2}d_3$$

Thus

$$P_Y = P_{\bar{X}_1 \bar{X}_2} d_0 + P_{\bar{X}_1 X_2} d_1 + P_{X_1 \bar{X}_2} d_2 + P_{X_1 X_2} d_3 \quad (13)$$

Eq.13 is nothing but the output probability P_y of a gate having two inputs X_1 and X_2 , and a truth table as in Figure (6-a).

The above result is useful since it establishes a duality between the Correlation Propagation Law and the gate's output probability. This duality is demonstrated below by comparing Eq.7,12 respectively. The equations are rewritten here for convenience :

$$R_{YA} = P_A d0 + R_{X1A} (d2-d0) + R_{X2A} (d1-d0) + R_{X1X2A}(d3+d0-d1-d2)$$

$$P_Y = d0 + P_{X1} (d2-d0) + P_{X2} (d1-d0) + P_{X1X2}(d3+d0-d1-d2)$$

The following duality is observed :

$$\begin{matrix} P_Y & \text{---} & R_{YA} & P_{X2} & \text{---} & R_{X2A} \\ 1 & \text{---} & P_A & P_{X1X2} & \text{---} & R_{X1X2A} \\ P_{X1} & \text{---} & R_{X1A} & & & \end{matrix}$$

Thus we may obtain the Correlation Propagation Law for a gate directly from its expression of output probability by exploiting the above mentioned duality.

2.3 Tools for Analyzing Circuits with Feedback

In circuits with feedback, an output of some stage is the input to a previous stage. In the block diagram of Figure (7-a), the combinational logic circuit has the inputs U_1, \dots, U_n and X , and an output Y which is fed back to a previous stage. To calculate the bias probability of X we need the bias probability of Y (and Z), but to obtain the latter we need to know the former. This subsection develops a method to calculate the bias probabilities of both Y and X .

Figure (7-b) represents the truth table of the combinational logic of Figure (7-a). It is required to find the bias probability of Y from the information given in the truth table.

The Total Probability Theorem states that [8] :

$$P\{Y\} = P\{Y|m_0\} P\{m_0\} + \dots + P\{Y|m_k\} P\{m_k\} \quad (14)$$

where m_0, \dots, m_k are partitions of the global event S . m_0, \dots, m_k in Eq. 14 are the minterms (rows) in the truth table of Figure (7-b). $P\{m_0\}, \dots, P\{m_k\}$ are the probabilities of these minterms, i.e. the probabilities of occurrence of the corresponding input patterns (U_1, \dots, U_n, X). $P\{Y|m_i\}$ is the probability that the output Y is 1, given that the input pattern is defined by minterm m_i . The output corresponding to the input pattern defined by minterm m_i may be easily obtained from the truth table. This output is either 1 or 0. Thus $P\{Y|m_i\}$ is 1 or 0 accordingly.

Removing from Eq. 14 the terms where $P\{Y|m_i\} = 0$, only those terms for which $P\{Y|m_i\} = 1$ remain. Thus Eq. 14 reduces to:

$$P_Y = \sum P\{Y|m_i\} P\{m_i\}, \text{ where } P\{Y|m_i\} = 1, \text{ i.e.}$$

$$P_Y = \sum P\{m_i\}.$$

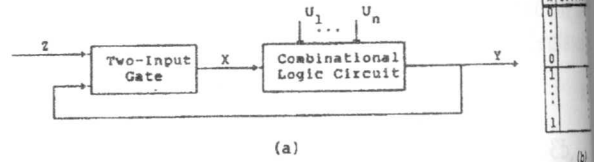


Figure 7. Analysis of circuits with feedback.

The above expression is the summation probabilities of all minterms m_i for which $Y=1$ in the truth table. All minterm probabilities have either a common factor P_X or $1-P_X$, since in any minterm there must be either \bar{X} or X .

Grouping the minterms in Eq. 15 into two groups containing \bar{X} and the other containing its complement X , we get:

$$P_Y = \sum P\{m_x\} + P\{m_{\bar{x}}\}$$

where :

$\sum P\{m_x\}$ is the probability sum of minterms with $X=1$.

$\sum P\{m_{\bar{x}}\}$ is the probability sum of minterms with $X=0$.

Minterm probabilities in the first group have the common factor P_X , while minterm probabilities in the second group have the common factor $1-P_X$, i.e. :

$$\sum P\{m_x\} = P_X H(u)$$

$$\sum P\{m_{\bar{x}}\} = (1-P_X) L(u)$$

where $H(u)$ and $L(u)$ are the subsets of $\sum P\{m_x\}$ and $\sum P\{m_{\bar{x}}\}$ respectively which are functions of inputs U_1, \dots, U_n only (and not X). They are given exclusively in terms of the probabilities of inputs U_1, \dots, U_n .

We therefore may express Eq. 16 as :

$$P_Y = P_X H(u) + (1-P_X) L(u)$$

where $H(u)$ and $L(u)$ are defined implicitly by Eq. 17. Alternatively, the total probability theorem may be rewritten as :

$$P_Y = P_X P \{Y|X\} + (1-P_X) P \{Y|\bar{X}\} \quad (19)$$

we conclude from Eq. 18 and 19 that :

$$\begin{aligned} H(u) &= P \{Y|X\}, \quad L(u) = P \{Y|\bar{X}\} \\ L(u) &= P \{Y|\bar{X}\} \end{aligned} \quad (20)$$

Thus to calculate $H(u)$ and $L(u)$ we may use Eq. 17 or 20.

Since X is the output of the gate in Figure (7-a), Y and Z are the inputs, P_X may be given by (see Eq. 12):

$$\begin{aligned} P_X &= d_0 + P_Z(d_2 - d_0) + P_Y(d_1 - d_0) \\ &+ P_{YZ}(d_3 + d_0 - d_1 - d_2) \end{aligned} \quad (21)$$

and since Y and Z are independent, we have $P_{YZ} = P_Y P_Z$. Substituting in Eq.21 we get :

$$\begin{aligned} P_X &= d_0 + P_Z (d_2 - d_0) + P_Y (d_1 - d_0) \\ &+ P_Y P_Z (d_3 + d_0 - d_1 - d_2) \end{aligned} \quad (22)$$

Substituting from Eq.22 into Eq.18 and solving for P_Y we finally obtain :

$$P_Y = \frac{L(u) + [H(u) - L(u)][d_0 + P_Z(d_2 - d_0)]}{1 - [H(u) - L(u)][(1 - P_Z)(d_1 - d_0) + P_Z(d_3 - d_2)]} \quad (23)$$

Eq.23,22 may be used to determine the probabilities of Y and X respectively as it will be shown in section 3. Eq. 23 will be extended to the multiple fan-in case in the next subsection.

2.4 Extension to Multiple Fan-In Circuits

In the previous subsections a set of tools were developed to deal with complex logic circuits. This subsection extends these tools to the case of multiple fan-in. By multiple fan-in it is meant that the gates

under consideration have more than two inputs. The following discussion assumes that a gate has a number n of inputs, where $n \geq 2$.

To extend theorem 1 to the multiple fan-in case, let the gate have the inputs X_1, \dots, X_n and one output Y . If all n inputs are independent then P_Y may be expressed in terms of P_{X_1}, \dots, P_{X_n} and 1 only. However, if subsets of the inputs are not independent then P may also depend on terms like $P_{X_i X_j}$, $P_{X_i X_j X_k}$ and so on until $P_{X_i X_j \dots X_n}$. The Correlation Propagation Law in such case is obtained by exploiting the duality principle. Thus to establish the Correlation Propagation Law for an n input gate, with inputs X_1, \dots, X_n and output Y , express its output bias probability P_Y as an algebraic sum of terms : 1 (e.g. in case of inverter), $P_{X_1}, \dots, P_{X_i \dots X_j}, \dots, P_{X_i X_j \dots X_n}$ (if they exist). Replace these terms by $P_A, R_{X_1 A}, \dots, R_{X_i \dots X_j A}, \dots, R_{X_1 X_2 \dots X_n A}$ respectively. The result is the output cross-correlation R_{YA} . The only restriction is that A must be a Boolean event. For example if :

$$P = 1 - P_{X_1 X_2 X_3 X_4} \quad (4\text{-input NAND})$$

By duality the Correlation Propagation Law is :

$$R_{YA} = P_A - R_{X_1 X_2 X_3 X_4 A}$$

In circuits with feedback (see Figure (7-a)), extension to multiple fan-in means that the gate has more than two inputs. This gate may then be decomposed into two separate gates as shown in Figure (8). Eq.23 is valid for gate 1. It gives the probability P_Y . The probability P_Z , however, is now interpreted as the output probability of gate 2. With this minor modification results of subsection 2.3 may be applied to gates with more than two inputs.

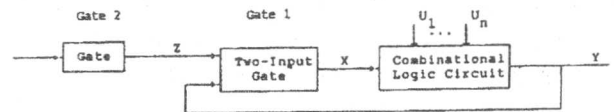


Figure 8. Analysis of multiple fan-in circuits.

3. ANALYSIS OF COMPLEX CIRCUITS

This section is organized as follows: Subsection 3.1 is devoted for analyzing the redundant tree topology,

subsection 3.2 analyzes the mesh structure, while subsection 3.3 is for analyzing circuits with feedback. The goals of the analysis in each of these sections are the following:

- 1- Find the probability transfer function of the circuit.
- 2- Determine the fixed point bias probability.
- 3- Calculate the path sensitization probability for a path extending from the input to the output of the circuit.
- 4- Determine the conditions which lead to the optimum (minimum) number of test generations M_{opt} .

3.1 Redundant Tree Topology

This subsection illustrates the effect of redundant fault detection. Consider the circuit in Figure 9. The structure shown is replicated at each level forming a redundant tree topology. Redundancy comes from the fact that l inputs are common to both OR gates at a level. Each OR gate also has its own m independent inputs. It is assumed that the probability of an independent input is P_u , and that of each common input is P_b . The output probability is P_{uo} . Note that Figure 9(a) is functionally equivalent to Figure 9(b).

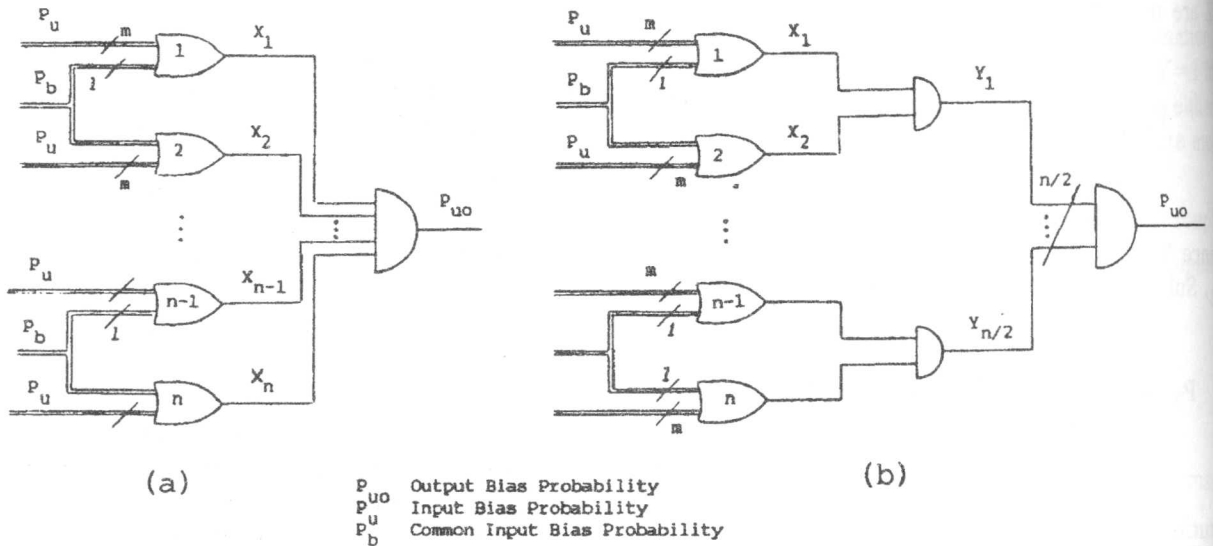


Figure 9. Redundant circuit topology.

The first step is to establish the probability transfer function for the circuit, i.e. an expression for P_{uo} in terms of P_u and P_b . The problem is that signals X_1 and X_2 are not independent since they have a common root. In such case, procedure 2 (subsection 2.2) must be invoked to determine $P_{X_1 X_2}$ which is needed to calculate P_Y (see Figure 9(b)).

First, define events A, B, C as :

A , at least one independent input to gate 1 is high.

B , at least one common input is high.

C , at least one independent input to gate 2 is high.

Since event $\{X_1=1\}$ is the ORing of events A and B, and event $\{X_2=1\}$ is the ORing of events B and C, the

redundant part of the circuit in Figure 9(b) may be redrawn as shown in Figure 10) which demonstrates the order in which the Correlation Propagation Law may be applied to the gates. This order is expressed in the form of successive steps.

Starting with the known statistics :

$$P_A = 1 - (1 - P_u)^m$$

$$P_B = 1 - (1 - P_b)^l$$

$$P_C = 1 - (1 - P_u)^m$$

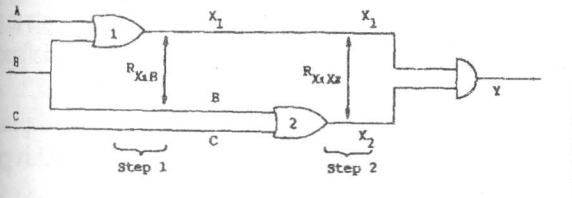


Figure 10. Use of the correlation propagation law.

We find the joint statistics of the corresponding signals, then in each subsequent step, one new signal is considered, and its associated joint statistics are calculated. This operation is repeated until the output signal is reached. Note that if events are independent, the calculation of the joint probability (statistics) is trivial, thus we shall calculate the joint probabilities of non independent events only.

At step 1 (see Figure (10)) signal X_1 is introduced. B and X_1 have a common root. Thus, they are non independent. Their joint probability is obtained by applying the Correlation Propagation Law as follows. The output probability of gate 1 is :

$$P_{X_1} = P_A + P_B - P_{AB} \quad (27)$$

It is desired to find P_{X_1B} . Applying the duality presented in subsection 2.2 with B as external event, we get :

$$\begin{aligned} R_{X_1B} &= P_{X_1B} = R_{AB} + R_{BB} - R_{ABB} \\ &= P_{AB} + P_B - P_{AB} = P_B \end{aligned} \quad (28)$$

At step 2 (see Figure (10)) X_2 is introduced. X_1 and X_2 have a common root. Their joint probability must again be determined by applying the Correlation Propagation Law. The output probability of gate 2 is :

$$P_{X_2} = P_C + P_B - P_{CB}$$

Since it is desired to find $P_{X_1X_2}$, apply Rule 1 of duality with X_1 as the external event. Thus we get :

$$R_{X_2X_1} = P_{X_2X_1} = P_{X_1X_2} = R_{CX_1} + R_{BX_1} - R_{CBX_1}$$

$$= P_C P_{X_1} + P_{BX_1} - P_C P_{BX_1}$$

Substituting for P_{BX_1} from Eq.28 we get :

$$P_{X_1X_2} = P_C P_{X_1} + P_B - P_C P_B = P_Y$$

Substituting for P_{X_1} from Eq.27 we get :

$$P_Y = P_C (P_A + P_B - P_A P_B) + P_B - P_C P_B,$$

thus:

$$P_Y = P_C P_A (1 - P_B) + P_B \quad (29)$$

Substituting from Eq.24-26 into Eq.29 we obtain :

$$P_Y = [1 - (1 - P_u)^m]^2 (1 - P_b)^\ell + 1 - (1 - P_b)^\ell \quad (30)$$

And referring to Figure (9) we get :

$$P_{uo} = \{ [1 - (1 - P_u)^m]^2 (1 - P_b)^\ell + 1 - (1 - P_b)^\ell \}^{n/2} \quad (31)$$

The above is the Probability Transfer Function of the circuit in Figure (9). It may be proved that it reduces to the transfer function of the pure tree structure developed in [4] (Eq.4), if redundant inputs were removed ($\ell=0$) or if their probabilities were set to 0 ($P_b=0$). By putting $\ell=0$ in Eq.31, we have $(1 - P_b)^\ell = 1$. Thus :

$$P_{uo} = \{ [1 - (1 - P_u)^m]^2 + 1 - 1 \}^{n/2} = [1 - (1 - P_u)^m]^n$$

which is the same as Eq.4. Also putting $P_b=0$ in Eq.31 we get $(1 - P_b)^\ell = 1$, thus the equation reduces again to Eq.4.

Once the probability transfer function is established, let us determine the fixed point bias probability involving the independent inputs (input probability P_u). It is assumed that each independent input is an output of a previous stage. By definition, its probability must be equal to that of the output at a fixed point [4]. The probability P_b of the common inputs may be regarded as a parameter describing the degree of redundancy. At a fixed point we have $P_{uo} = P_u$. Substituting for P_{uo} from Eq.31 we get :

$$P_u = \{ [1 - (1 - P_u)^m]^2 (1 - P_b)^\ell + 1 - (1 - P_b)^\ell \}^{n/2} \quad (32)$$

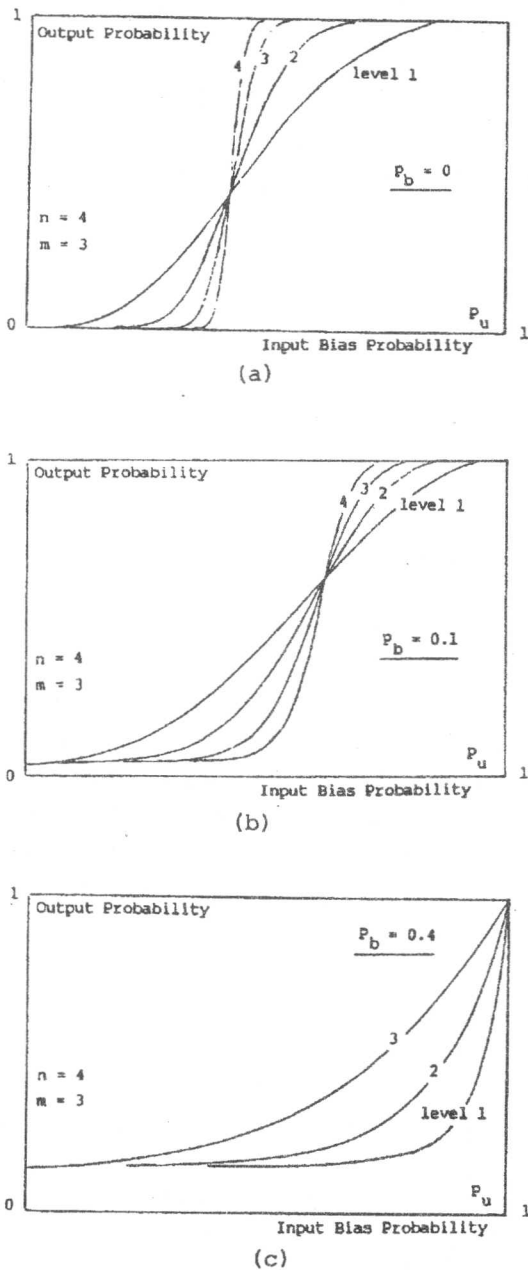


Figure 11. Effect of P_b and on the fixed point.

The fixed point bias probability is the solution of Eq.32 for P_u . If the equation has no solution then the fixed point does not exist. If it has a solution then the fixed point exists and its bias probability is P_u . Figure (11-a), ..., (11-c) demonstrate that the existence of the fixed point largely depends on the values of ℓ and P_b .

The next step is to find path sensitization probability for the path extending from an input of the first level

to an output from the last level. Consider the circuit in Figure (9). Let one of the m independent inputs to gate 1 be the faulty one. Also, let event A' be defined as follows :

A' , at least one of the $m-1$ not faulty independent inputs to gate 1 is high. The probability of A' is given by :

$$P'_{A'} = 1 - (1-P_u)^{m-1}$$

Let events B and C be as defined before in Eq.25. From Figure (9), it may be concluded that a fault on the input of the OR gate propagates to the output P_{uo} if and only if events A' and B do not occur and event C occurs. i.e. sensitization $\bar{A}' \bar{B} C$. Thus,

$P_{S1} = P'_{A'} P'_{\bar{B}} P_C = (1 - P_{A'}) (1 - P_B) P_C$, where P_{S1} is the probability of sensitizing the path to the output P_{uo} in Figure (9). Substituting from Eq.25,26,33 we get:

$$P_{S1} = (1-P_u)^{m-1} (1-P_b)^\ell [1-(1-P_u)^m]$$

Note that signal Y could still be masked from the output P_{uo} if any of the other $n/2-1$ inputs to the second AND gate in Figure (9) is low. This means that these $n/2-1$ inputs must be high in the case of path sensitization. The probability of this event may be obtained by substituting $n/2-1$ instead of $n/2$ in Eq.

$$P_{S2} = P_{S1} [[1-(1-P_u)^m]^2 (1-P_b)^\ell + 1-(1-P_b)^\ell]^{n/2-1}$$

Where P_{S2} is the probability of sensitizing a path to the output P_{uo} . The probability of sensitizing a path through k levels, denoted by P_s , is:

$$P_s = (P_{S2})^k$$

Eq. 34-36 determine the path sensitization probability P_u is obtained by solving Eq. 32.

The following results summarize the extension of fault detection techniques to the adopted redundant circuit structure:

- 1- The number of test generations necessary to assure that the circuit is error free with probability P_s

given by (Eq. 1):

$$M = \frac{\log(1-P)}{\log(1-P_s)} \text{ where, } P_s \text{ is defined by Eq.34-36.}$$

- 1- The test length is optimum ($M=M_{opt}$) when P_u is the fixed point probability obtained by solving Eq. 32.
- 2- The system has a fixed point if Eq. 32 has a real solution.

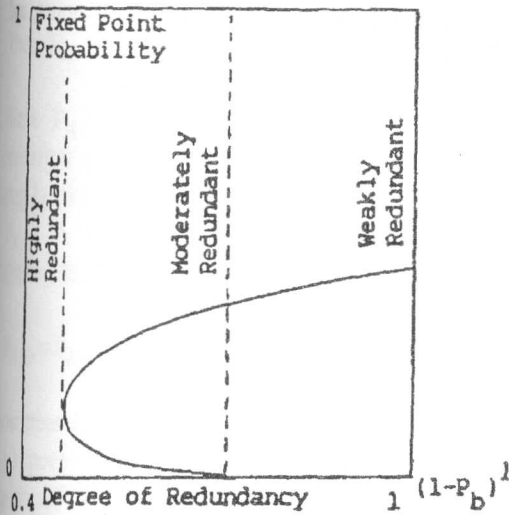


Figure 12. Fixed point probability versus degree of redundancy.

In eq. 32 the term $(1-P_b)^\ell$ may be viewed as the effect of redundancy. In non redundant circuits ($P_b=0$ or $\ell=0$) this term equals 1. As the degree of redundancy increases (ℓ approaches infinity or P_b^ℓ approaches 1) the term approaches zero. Thus the smaller the term $(1-P_b)^\ell$ is, the more redundant is the circuit. Figure (12) shows the fixed point probability (the solution of Eq. 32) versus the degree of redundancy $(1-P_b)^\ell$. It is to be noted that for highly redundant circuits (low $(1-P_b)^\ell$) the fixed point does not exist. For circuit of moderate redundancy there are two fixed points. Finally for weakly redundant circuits (including the nonredundant case where $(1-P_b)^\ell = 1$) there is one fixed point only.

4- Redundant circuits are generally more difficult to test for correctness. The following paragraphs

explain this conclusion.

Consider the highly redundant circuits, where no fixed points exist. In such case there is no input probability P_u to satisfy $P_{uo} = P_u$, where P_{uo} is given by Eq.31. This means that either $P_{uo} > P_u$ for all values of P_u , or $P_{uo} < P_u$ for all values of P_u . Noting that the output P_{uo} of level i is the input P_u of level $i+1$, one concludes that if there is no fixed point, then either $P_u(i+1) > P_u(i)$ for all i , or $P_u(i+1) < P_u(i)$ for all i . Taking the limit as i tends to infinity we get either $P_u(\infty)=1$, or $P_u(\infty)=0$. In both cases the path sensitization probability P_s (see Eq. 34-36) is zero. This means that the path from the faulty gate to the circuit output is never sensitized. Thus, the random testing technique fails. Note that putting $P_s = 0$ in Eq.1 gives $M = \infty$. This leads to the conclusion, that highly redundant circuits may not be amenable to random testing.

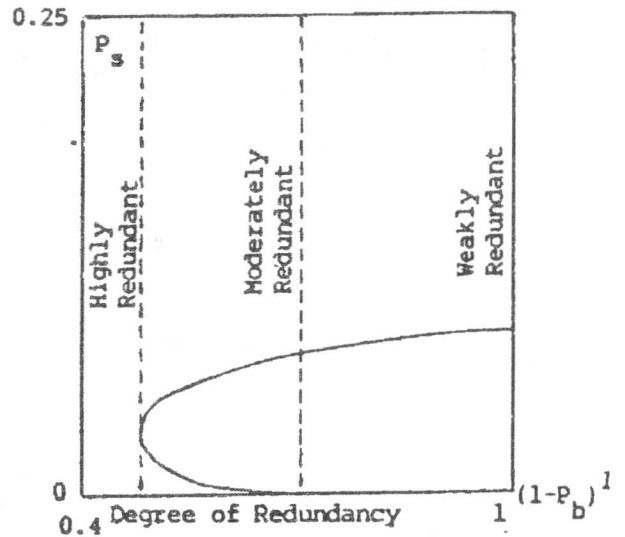


Figure 13. Path sensitization probability versus degree of redundancy.

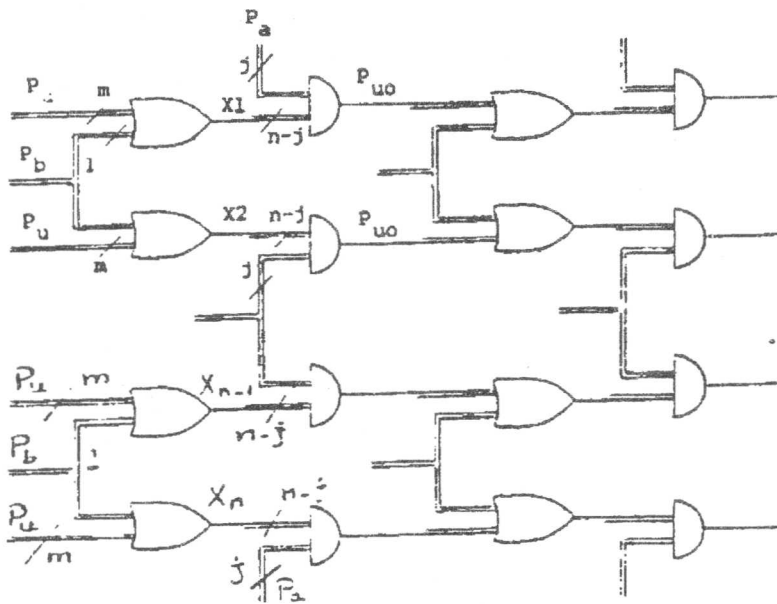
Now consider moderately redundant circuits. Figure (13) demonstrates the path sensitization probability of one level (Eq. 34, 35) versus the degree of redundancy $(1-P_b)^\ell$. Note that the sensitization probability increases as the degree of redundancy decreases i.e. as $(1-P_b)^\ell$ approaches 1. Thus it is easier to sensitize a path in a non redundant circuit and therefore less tests are

required (see Eq. 1). Therefore redundant circuits are more difficult to test for correct operation than their non redundant counterparts.

The following rule applies to all redundant circuits : To achieve the minimum (limited) test length, try to select the inputs in such a way as to reduce circuit redundancy. To reduce redundancy set all (most) lines common to several OR gates to 0, which means that their bias probabilities are 0 (slightly higher than zero), and set all (most) lines common to several AND gates to 1, which means that their bias probabilities are 1 (slightly lower than 1).

3.2 Mesh Topology

This subsection extends circuit structure to the mesh topology. Consider the circuit in Figure (14). There are ℓ external inputs common to each pair of OR gates and j external inputs common to each pair of AND gates. All external inputs are mutually independent. Each OR gate also has its own m independent inputs. Each AND gate has a total fan in of n . P_u , P_b , and P_{uo} refer to the probabilities of independent inputs, external OR inputs, external AND inputs, and output (see Figure (14)).



- P_u Input Bias Probability
- P_{uo} Output Bias Probability
- P_b Common Input Probability
- m No. of Independent OR inputs
- l No. of Common OR inputs
- j No. of Independent AND inputs
- n AND gate fan-in.

Figure 14. Mesh circuit topology.

The first step towards the analysis of such circuit is to establish its probability transfer function, i.e. an expression for P_{uo} in terms of P_u , P_b and P_a . From Figure (14) it may be proved that :

$$P_{X1} = P_{X2} = 1 - (1-P_b)^\ell (1-P_u)^m, \text{ thus :}$$

$$P_{uo} = P_a^j [1 - (1-P_b)^\ell (1-P_u)^m]^{n-j} \quad (37)$$

where $X1$ and $X2$ are shown in Figure (14).

Eq. 37 gives the probability transfer function of single module, which is the relation between the input bias probability (denoted by P_u) of a module and its output bias probability (denoted by P_{uo}). Note that eliminating redundancy by making $\ell = j = 0$ (i.e. deleting all lines labeled ℓ or j from Figure (14)), Eq. 37 reduces to:

$$P_{uo} = [1 - (1-P_u)^m]^n$$

which is the same as Eq.4. Thus the redundant mesh structure may reduce to the nonredundant tree structure described in [3] and [4].

The last equation may also be proved using the correlation propagation laws (section 2.2). Figure (15-a) shows a simplified part of Figure (14), from which P_{uo} may be calculated. Events A and B, are as defined in section 3.1, and event D is defined as follows.

D, all j external AND gate inputs are high.

$$\text{Thus } P_D = P_a^j \quad (39)$$

Since $P_{X1} = P_A + P_B - P_{AB}$, applying the correlation propagation law with the external event being D, we get :

$P_{X1D} = P_{AD} + P_{BD} - P_{ABD}$, and since B is independent, we have:

$$P_{X1D} = P_{AD} + P_B P_D - P_B P_{AD} = P_{AD} + P_B (P_D - P_{AD}).$$

Now note that the AND gate in Figure (15-a) still has n-j-1 more inputs like X1, apart from the input D and the input X1 considered above. Thus its output probability P_{uo} may be expressed by :

$$P_{uo} = P_{X1}^{n-j-1} P_{X1D}. \text{Substituting from above this gives:}$$

$$P_{uo} = (P_A + P_B - P_{AB})^{n-j-1} [P_{AD} + P_B (P_D - P_{AD})],$$

and since B is independent, the above expression reduces to :

$$P_{uo} = [P_A + P_B (1 - P_A)]^{n-j-1} [P_{AD} + P_B (P_D - P_{AD})], \quad (40)$$

Eliminating redundancy by making $\ell = j = 0$, Eq. 40 must reduce to Eq. 38. To demonstrate it, note that setting $\ell = 0$ makes $P = 0$ (Eq. 25), and setting $j = 0$ makes $P_D = 1$ (Eq. 39). Thus Eq. 40 reduces to :

$$P_{uo} = P_A^{n-j-1} P_{AD}$$

but since $P_D = 1$, event D is a sure event (given $j = 0$), from which :

$P_{AD} = P\{(\text{Event A}) \text{ and } (\text{The Sure Event})\} = P_A$. Thus we get:

$$P_{uo} = P_A^{n-j-1} P_A = P_A^n \text{ (note that } j = 0 \text{.)}$$

finally substituting for P_{uo} from Eq. 24, the expression for P_{uo} becomes :

$$P_{uo} = [1 - (1 - P_a)^m]^n$$

which is the same as Eq. 38.

It should be noted that while the probability of each output is P_{uo} , the joint probability of two outputs is not P_{uo}^2 since they are correlated. The correlation propagation law may be employed to obtain this joint probability. To demonstrate how this may be done consider Figure (15-b) which shows a part of the mesh in Figure (14), which is redrawn to facilitate later analysis. Events A, B and C, relating to gates 1 and 2 are as defined in section 3.1. For generality, it is assumed that A and C are correlated. The solution is carried out on four steps.

First, since $P_{X1} = P_A + P_B - P_{AB}$, from duality, with B being the external event, we get $R_{X1B} = R_{AB} + R_{BB} - R_{ABB}$, thus $P_{BX1} = P_{AB} + P_B - P_{AB} = P_B$. Similarly, with C the external event we get $P_{CX1} = P_{AC} + P_B P_C - P_B P_{AC}$, and with CX1 the external event we may prove that $P_{BCX1} = P_B P_C$.

Second, Since $P_{X2} = P_B + P_C - P_{BC}$, from duality, with X1 being the external event, we obtain $P_{X2X1} = P_{BX1} + P_{CX1} - P_{BCX1}$. Substituting for the terms in the right hand side from the expressions obtained in the previous step we may prove that $P_{X1X2} = P_B + (1 - P_B) P_{AC}$.

Third, since $P_{Y1} = P_a^j P_{X1}$, we have

$$P_{Y1X2} = P_a^j P_{X1X2},$$

Fourth and last, since $P_{Y2} = P_a^j P_{X2}$, we have :

$$\begin{aligned} P_{Y1Y2} &= P_a^j P_{Y1X2} = P_a^{2j} P_{X1X2} \\ &= P_a^{2j} [P_B + (1 - P_B) P_{AC}] \quad (41) \end{aligned}$$

This is the expression for joint output probability.

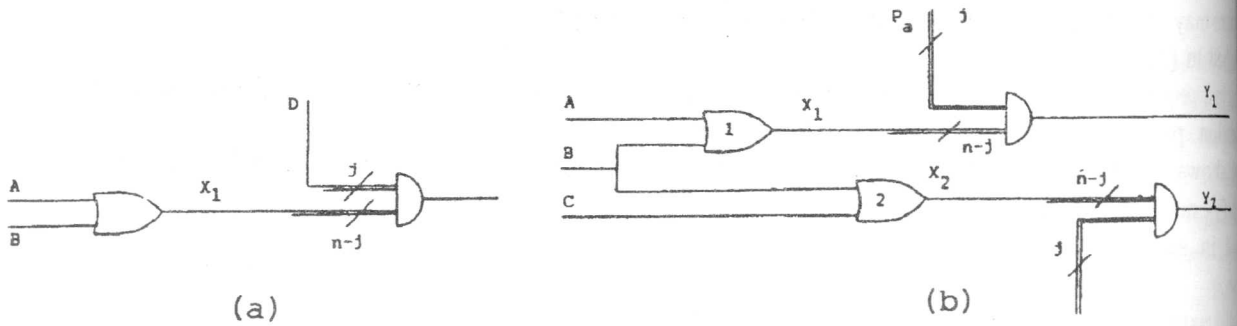


Figure 15. Analysis of mesh circuits.

The next step is to find path sensitization probability from an input to the first level to an output of the last. Using Boolean logic, and the definition of the probability of an event, it can be proved that path sensitization probability from a module input to X1 and Y1 (see Figure (14)), denoted by P_{S1} , P_{S2} respectively are given by the following equations :

$$P_{S1} = (1-P_b)^\ell (1-P_u)^{m-1} \quad (42)$$

$$P_{S2} = P_{S1} P_a^j [1 - (1-P_b)^\ell (1-P_u)^m]^{n-j} \quad (43)$$

and finally the path sensitization probability P_s of k levels is :

$$P_s = (P_{S2})^k \quad (44)$$

The input bias probability P_u must be the fixed point probability given by solving Eq.41 with $P_{uo} = P_u$ for P_u . It is given by :

$$P_u = P_a^j [1 - (1-P_b)^\ell (1-P_u)^m]^{n-j} \quad (45)$$

The main conclusions about fault detection in the proposed mesh structure may be outlined as follows :

- 1- The number of test generations necessary to assert that the circuit is error free with probability P is given by :

$$M = \log (1-P) / \log (1-P_s) \text{ (see Eq. 1)}$$

where P_s is defined in Eq. 42-44.

- 2- The condition which leads to the optimum test length M_{opt} is that P_u has to be the fixed point bias probability obtained by solving Eq. 41 for P_u .

- 3- As it has been in the previous subsection, the term $(1-P_b)^\ell$ in Eq. 41-44 is viewed as the effect of redundancy, the term P_a^j is the effect of having external inputs at each level of the mesh. The existence of external inputs at each level characterizes the mesh structure, since any cascaded levels in the mesh may be combined into one level only, unless there are external inputs to the second stage which are not inputs to the first. Since external inputs are always present at each level of a mesh, understanding their effect on fault detection is a basic issue in circuit analysis.
- 4- The effect of external inputs on test length : The system has a fixed point if Eq. 45 has a solution for P_u . Figure (16) shows the fixed point probability for five different values of P_a . Each curve is a plot of the solutions of Eq. 45 for a fixed value of P_a versus $(1-P_b)^\ell$.

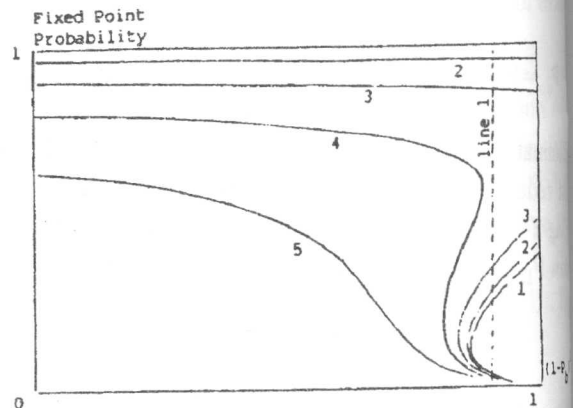


Figure 16. Fixed point probability versus degree of redundancy.

Note that putting $P_a = 1$ eliminates the effect of external inputs on P_u (the term P_a^j disappears from Eq. 45). With no external inputs ($j=0$), the curve has the same shape as in Figure (12) for tree structure. The characteristics of the mesh structure reduce to that of a tree.

As P_a decreases slightly (e.g. curve 2 and 3 in Figure (16)), another root appears to Eq. 45 (see the upper part of Figure (16), for curves 2, 3, for a given value of $(1-P_b)^l$). This means that the introduction of external inputs creates a new fixed point.

As P_a decreases a bit more (curve 5 in Figure (16)), the old fixed point gradually disappears. Note that any vertical line may intersect curve 5 in no more than one point. Recall that curves 2 and 3 may be intersected in more than one point. Thus the effect of external inputs is introducing a new fixed point and eliminating the old one.

Figure (17) plots the path sensitization probability (Eq. 44) versus $(1-P_b)^l$. Curve 1 is plotted for $P_a=0.98$, curve 2 is plotted for $P_a=0.95$. They correspond to curves 2 and 3 respectively in Figure (16). From Figure (16) note that for moderate redundancy each curve has two fixed points, one of which is created by the presence of external inputs. Path sensitization probability at that fixed point is much less than that at the original one (e.g. B1, C1). Less path sensitization probability means longer testing time.

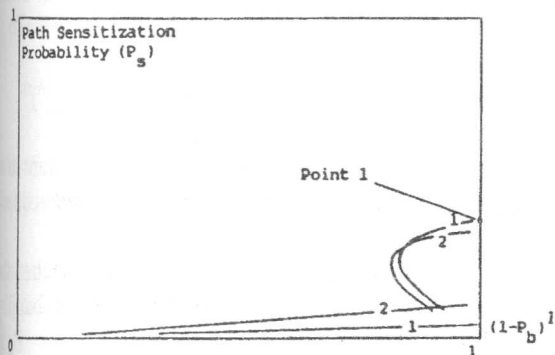


Figure 17. Path sensitization probability versus degree of redundancy.

Note also that the maximum path sensitization probability is achieved at point 1 of curve 1 (see Figure (17)), where curve 1 corresponds to $P_a=0.98$ (nearly 1), which means that the effect of external inputs is minimum, and point 1 corresponds to

$(1-P_b)^l = 1$, which is the nonredundant case.

Thus, to minimize test length (i.e. the number of generated input patterns) it is desired to select the input bias probabilities such that redundancy is minimum, which is consistent with the conclusion made in subsection 3.1, also external inputs must have minimum effect, which is achieved by setting $P_a=1$. The input bias probability of inputs to the first level is the fixed point probability. If there are two fixed points neglect the one created by the presence of external inputs, it corresponds to smaller path sensitization probability.

3.3. Circuits with Feedback

Feedback is isolated from other factors which may affect the analysis, namely, the degree of circuit redundancy and the number of external inputs. To achieve this isolation simple non redundant tree structure has been chosen, and a feedback loop has been added, as shown in Figure (18-a). In this structure each AND gate has n inputs except for the AND gate involving the feedback signal which has $n+1$ inputs. Also each OR gate has m inputs, $m-1$ of which do not involve feedback. Input bias probability of a stage is denoted by P_u and output bias probability is denoted by P_{uo} . The feedback loop has an Enable signal e , which has a bias probability P_e . The effect of the feedback loop may be increased or decreased by changing the bias probability of the Enable signal e . As P_e increases the effect of the feedback loop decreases and vice versa.

To analyse the circuit of Figure (18-a) Let us define event Z as :

$Z = \{ \text{All } n \text{ non-feedback inputs of the AND gate are high} \}$.

Thus
$$P_Z = P_u^n \tag{46}$$

Now, redraw the feedback loop in a manner consistent with the model presented in Subsection 2.3 (see Figure (18-b)).

The Gate block in Figure (18-b) has the truth table shown in Figure (19-a). The combinational logic block has the truth table shown in Fig. 19-b. The probability P_Y is given by Eq.23 (see subsection 2.3 for complete derivation):

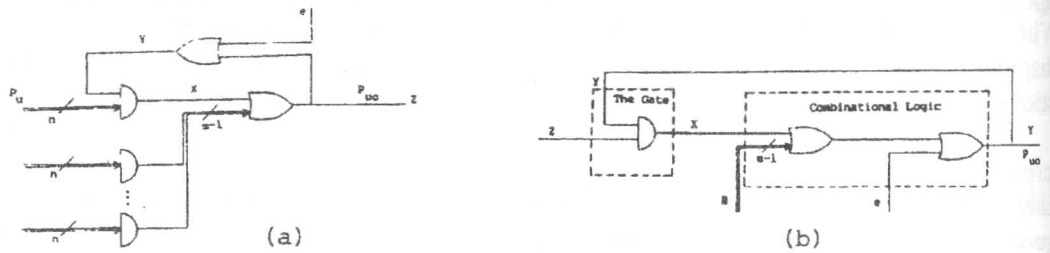


Figure 18. Analyzed circuit with feedback.

Z	Y	X
0	0	0
0	1	0
1	0	0
1	1	1

(a)

X	B	e	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

Figure 19. Truth tables of the analyzed circuit.

$$P_Y = \frac{L(u) + [H(u) - L(u)][d_0 + P_Z(d_2 - d_0)]}{1 - [H(u) - L(u)][(1 - P_Z)(d_1 - d_0) + P_Z(d_3 - d_2)]}$$

Comparing the truth table in Figure (19-a) with that in Figure (6) (see subsection 2.3) we get :

$$d_0 = d_1 = d_2 = 0, d_3 = 1. \quad (47)$$

And from the truth table in Figure (19-b), we have:

$$H(u) = 1 \quad (48)$$

$$L(u) = 1 - (1 - P_u^n)^{m-1} (1 - P_e) \quad (49)$$

where H(u) and L(u) are defined in Eq. 17 (subsection 2.3). Substituting in Eq. 23 from Eq. 47-49, we get :

$$P_Y = \frac{1 - (1 - P_u^n)^{m-1} (1 - P_e)}{1 - (1 - P_u^n)^{m-1} (1 - P_e) P_u^n} \quad (50)$$

$$\text{and } P_X = P_{YZ} = P_Y P_Z = P_Y P_u^n$$

$$= \frac{1 - (1 - P_u^n)^{m-1} (1 - P_e)}{1 - (1 - P_u^n)^{m-1} (1 - P_e) P_u^n} P_u^n \quad (51)$$

We also have (see Figure (18)):

$$P_{uo} = 1 - (1 - P_X) (1 - P_u^n)^{m-1} \quad (52)$$

Combining Eq. 51, 52 we get the probability trans function:

$$P_{uo} = 1 - \left[1 - \frac{(1 - P_u^n)^{m-1} (1 - P_e)}{1 - (1 - P_u^n)^{m-1} (1 - P_e) P_u^n} P_u^n \right] (1 - P_u^n)^{m-1}$$

As a verification note that putting $P_e = 1$ in Eq. 51 terms $(1 - P_e)$ become zero. The equation reduces to

$$P_u = 1 - (1 - P_u^n) (1 - P_u^n)^{m-1} = 1 - (1 - P_u^n)^m$$

which is the same as Eq. 4 for non redundant structure derived in [4]. Thus the effect of feedback disappears when $P_e = 1$.

The circuit in Figure (18) has a fixed point when output probability P_{uo} is equal to the input probability P_u . To find the fixed point probability set $P_{uo} = P_u$ in Eq. 53 and solve for P_u . Figure (20) shows the output and fixed point bias probabilities of the first five levels of the circuit for largely different values of P_e . From Figure (20) it is evident that the introduction of feedback loop changes slightly the fixed point bias probability. Note that increasing P_e from 0.2 to 1.0 by 500% changes the fixed point bias probability by less than 5%. Such change may be practically neglected.

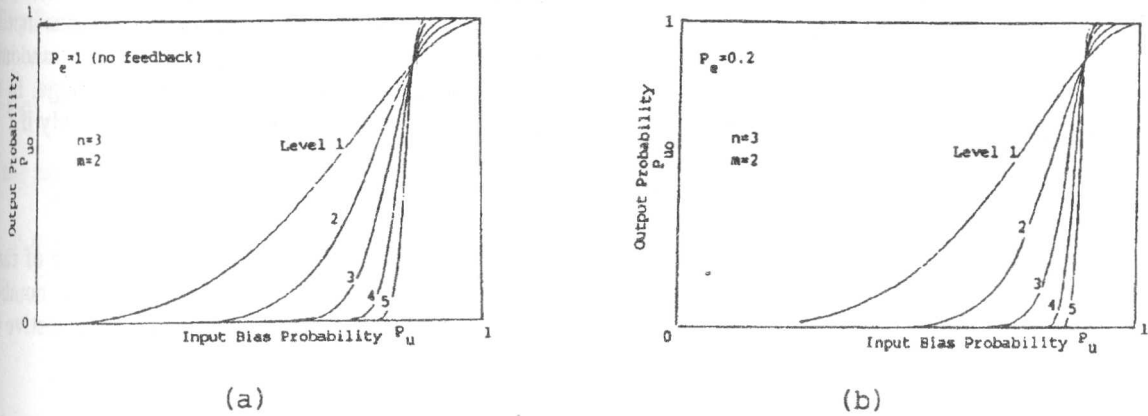


Figure 20. Output probability versus input bias probability.

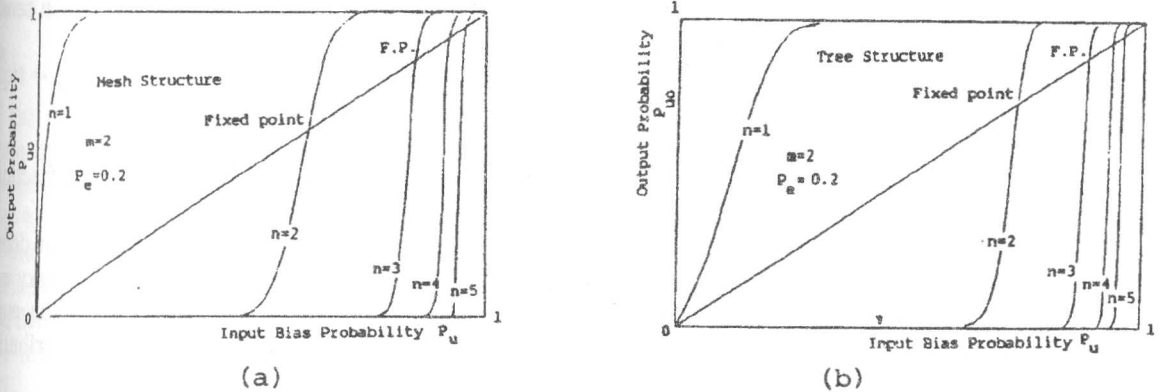


Figure 21. Effect of changing fan-in on fixed point probability.

Figure (21) Shows the effect of changing fan-in on fixed point probability. In Figure (21-a) the output bias probability of the 5th level and the fixed point probability are shown for different AND gate fan-in's. These values are compared with the corresponding ones for pure tree structure (Figure (21-b), note $P_e=1$). No appreciable difference is observed.

The following may be concluded :

- 1- The presence of feedback does not alter appreciably the fixed point probability of the module in which the feedback loop is present. Thus to simplify the analysis, feedback loops may be neglected. Indeed the feedback does not add any new elements or inputs to the circuit, and therefore does not contribute very much to simplifying or complicating the process of fault detection.

From Figure (18-a) note that if X is stuck (at '1' or

'0'), the probability that the fault is propagated to the output Z is the same as that for pure tree structure. This is because the remaining part of the circuit (i.e. that which functions correctly) is the same as that of a pure tree. Thus the path sensitization probability of the path extending from X to the output Z of the module containing the faulty element is the same for both cases.

- 2- The fan-in has a more pronounced effect on fixed point probability (Figure (21)). Increasing the fan-in moves the fixed point in the direction which decreases the path sensitization probability and thus increases test length. It is understood that the fan-in cannot be varied during circuit testing since it is determined by the given circuit design and is not a test signal parameter. Therefore if fan-in is high, the penalty on test length has to be accepted as a

fact which cannot be avoided. Thus, increasing fan-in prolongs the testing process (fault detection).

Note that as fan-in increases (Figure (21)) the fixed point probability becomes nearly unity. In a simple tree structure, for example, the sensitization probability of one level is given by (see [4]) :

$$P_{SI} = P_u^{n-1} (1 - P_u^n)^{m-1}$$

As P_u tends to 1, the above expression tends to 0, which means that the test length M (see Eq. 1) increases. Since feedback does not alter the fixed point too much, the same result applies for circuits with feedback. It can be shown that this result also applies for redundant and mesh structures. Eq.34-36 and Eq.42-44 give path sensitization probabilities for redundant circuits and mesh circuits respectively. Substituting with $P_u=1$ in these equations results in a path sensitization probability $P_s=0$.

4. RANDOM VERSUS EXHAUSTIVE TESTING :

In this section a mathematical expression will be derived to indicate whether it is better to use random testing or it is better to use exhaustive testing. For circuit with few inputs, say 2 or 3 inputs, the exhaustive testing is quite simple (2^2 or 2^3 patterns respectively). Thus there is no need to resort to random testing. As the number of inputs increases, exhaustive test length grows exponentially. At some point it becomes more practical to use a random test. The purpose of the coming discussion is to find an expression for the critical number of inputs beyond which the random test is recommended, and relate this expression to circuit parameters. After an exhaustive test is performed, one knows with absolute certainty whether the circuit is fault free or not. On the other hand, after a random test is performed one is never absolutely sure. All the random test can guarantee is a probability P that the circuit is error free. Although this probability P can be made arbitrary close to 1, it can never be exactly equal to 1, since in that case the required test duration M must be infinite as predicted by Eq.1 (rewritten below).

$$M = \log(1-P) / \log(1-P_s)$$

and for $P=1$, $M = \log(0) / \log(1-P_s)$

If no faults are discovered during a random test, the

circuit could still be faulty since the pattern which sensitizes the path to the faulty gate has not been applied. Thus one should not select the random test unless the time savings are sufficiently large. In other words the random test is recommended only if :

$$M_{rand} < k.M_{exhaust}, \quad k \ll 1,$$

where :

- k is the ratio between the number of random test generations and the total number of generations needed for an exhaustive test.
- $M_{exhaust}$ is the exhaustive test length.
- M_{rand} is the random test length.

It is now desired to relate Eq. 54 to the number of circuit inputs.

Let $q = 2^r$ denote the number of all possible input patterns, where r is the number of inputs.

Let t be the number of input patterns which sensitizes the path to the faulty gate.

This path sensitization probability P_s is $P_s = t/q$, the number of random patterns applied be:

$$M_{rand} = b.q, \text{ where } b \text{ is some arbitrary fraction}$$

Since each applied pattern either sensitizes or does not sensitize the path, it may be viewed as a binary event. Thus the probability that a number x of the applied patterns sensitize the path has a binomial distribution

$$P \{Sensit. = x\} = \binom{b.q}{x} P_s^x (1-P_s)^{b.q-x}$$

If path sensitization probability P_s , and the number of applied random patterns $b.q$ are such that

$P_s \ll 1$, and $b.n \gg 1$, which is typically the case, then Poisson theorem states that the Binomial distribution (Eq. 55) tends to a Poisson distribution with parameter $P_s.b.q$. Thus :

$$P \{Sensit. = x\} = e^{-P_s.b.q} \frac{(P_s.b.q)^x}{x!}$$

The probability P that at least one pattern sensitizes the path is :

$$P = 1 - P \{Sensit. = 0\}$$

Substituting for x by 0 in Eq. 56, and inserting in Eq. 57 we get:

$$P = 1 - e^{-P_s.b.q}$$

If it is desired that the circuit be error free with a probability $P=99.9\%$, i.e $P=0.999$, then from Eq. 58:

$$0.999=1-e^{-P_s \cdot b \cdot q} \text{ from which } 0.001 = e^{-P_s \cdot b \cdot q}$$

Taking the natural logarithm of both sides we get :

$$P_s \cdot b \cdot q \approx 7, \text{ where by definition } q = 2^r .$$

$$\text{Thus } b = \frac{M_{\text{rand}}}{M_{\text{exhaust}} 2^r \cdot P_s} = \frac{7}{2^r \cdot P_s} \quad (59)$$

Finally, combining Eq. 54 and 59 we get the condition for applying the random test method. The random test may be applied only if :

$$7 / (2^r \cdot P_s) < k \quad (60)$$

where :

P_s is the path sensitization probability as obtained from the equations of the corresponding circuit structure (e.g. Eq. 34-36 for redundant structure, Eq. 42-44 for mesh structure).

k is the required time saving of the random test, defined by inequality (54). For example if it is required that the random test take no more than 0.1 the time an exhaustive test takes, then $k = 0.1$.

5. CONCLUSIONS

In this section the conclusions of this study are summarized, their significance and physical implications are outlined.

5.1 About Redundant Structures

Redundancy in logic circuits is one of the factors contributing to increasing circuit test duration. This effect is expected since redundancy is often introduced for fault tolerance, and fault tolerance aims at hiding faults within the circuit such that they do not affect its outputs. Thus, discovering such hidden faults becomes more difficult, and requires a longer test. In Figure (13) the maximum path sensitization probability is obtained in a nonredundant circuit. As the degree of redundancy increases the path sensitization probability decreases which means that faults become more

difficult to discover. The expression for path sensitization probability P_s is given by Eq. 34-36. The corresponding number of test generations is given by Eq. 1.

To minimize the number of test generations, the following conditions must be observed :

- For inputs common to several OR gates, set the input bias probability to 0.
- For inputs common to several AND gates, set the input bias probability to 1.

The above conditions reduce the degree of redundancy. In addition the following must be observed :

- The optimum bias probability of the input signals to be applied during testing is calculated by solving Eq. 32. It should be noted that for highly redundant circuits, Eq. 32 has no solution (see Figure (12)), and the random testing approach fails. Highly redundant circuits therefore may not be amenable to random testing.

5.2 About Mesh Structures

Mesh structures usually have external inputs at each level. In section 3.2 it has been proved that the existence of these external signals shifts the circuit fixed point in a direction which reduces path sensitization probability (see Figures (16), (17)). This means that the number of required test generation increases. Path sensitization probability P_s for mesh structures is given by Eq. 42-44. The corresponding number of test generations is given by Eq. 1. The test length M is minimum when the input bias probability P_u is the solution of Eq. 45. This equation may have more than one solution for P_u . In such case one should select P_u which corresponds to the larger path sensitization probability. Figures (16), (17) may be useful in that selection.

In redundant mesh structure the effect of external inputs must be minimized by setting their probabilities to 1 (0) if they enter AND (OR) gates. This maximizes path sensitization probability.

5.3 About Feedback

The presence of feedback does not alter appreciably the fixed point probability of the module in which the

feedback is present. Accordingly, the path sensitization probability is almost insensitive to feedback, which has an important implication. It means that feedback loops may be neglected in circuit analysis as far as only fault detection is concerned. Feedback does not add any new elements or inputs to the circuit, and thus does not contribute much to simplifying or complicating the process of fault detection (Figures (20), (21)).

5.4 About Fan-in

Although the effect of fan-in has not been studied separately in a section of its own, the fan-in has been included as an explicit parameter in all derived equations for path sensitization probabilities and fixed point probabilities for the different circuit topologies.

It has been observed that fan-in has a large effect on fixed point probability. Increasing the fan-in moves the fixed point in the direction which decreases path sensitization probability and thus increases test length. This effect is clearly demonstrated in Fig. 21 where the increase in AND gate fan-in moves the fixed point very close to 1, which significantly decreases path sensitization probability P_s (see Eq. 34-36, 42-44). Notice that when $P_u = 1$, we get $P_s = 0$. Another manifestation of the same effect may be observed in Figures (13) and (17), which plot path sensitization probability for the circuits in Figures (9) and (14) respectively versus the degree of redundancy $(1-P_b)^\ell$. Notice that increasing ℓ (which means increasing OR gate fan-in) decreases the value of $(1-P_b)^\ell$ and thus decreases path sensitization probability as evident from Figures (13) and (17). This result has an obvious explanation. As the number of inputs increases, it becomes more and more difficult to find the input pattern which sensitizes some given path. Therefore, path sensitization probability decreases.

Unfortunately, nothing can be done to improve test length if the circuit has a large fan-in. Fan-in cannot be reduced during testing, since the only way to reduce it is by cutting some connections between gates. This is something like destroying the circuit in order to test it for correctness.

5.5 The Applicability Conclusion

Random testing should not be applied, unless the applicability condition (inequality (60)) is satisfied for the circuit at hand. If it is not satisfied, then the exhaustive testing is better.

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